

Logic Diagram

FEATURES:

- 32K x 16 Bit OTP EPROM organization
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
 - > 100 Krad (Si), depending upon space mission
- Excellent Single Event Effects:
 - SEL_{TH} LET: > 80 MeV/mg/cm²
 - SEU_{TH} LET: > 80 MeV/mg/cm²
- Package:
 - 40 pin RAD-PAK® DIP
- Low power consumption:
 - Active mode: 500 mW @ 10 MHz
 - Standby mode: < 11 mW
- High speed page and word programming:
 - Page programming time: 14 sec (typ)
- Programming power supply:
 - V_{pp} = 12.5 V ± 0.3 V
- One-time Programmable
- Pin Arrangement
 - Flash memory and mask ROM compatible

DESCRIPTION:

Maxwell Technologies' 27C1512T high density 512K OneTime Programmable Electrically Programmable Read Only Memory multi-chip module (MCM) features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 27C1512T features fast address times and low power dissipation. The 27C1512T offers high speed programming using page programming mode.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defined Class K.

TABLE 1. 27C1512T PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
21-29, 31-36	A0 - A14	Address
19-12, 10-3	I/O0 - I/O15	Input/Output
2	\overline{CE}	Chip Enable
20	\overline{OE}	Output Enable
40	V _{CC}	Power Supply
1	V _{PP}	Programming Supply
11, 30	V _{SS}	Ground
39	\overline{PGM}	Programming Enable
37, 38	NC	No Connection

TABLE 2. 27C1512T ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage ¹	V _{CC}	-0.6	7.0	V
Programming Voltage ¹	V _{PP}	-0.6	13.5	V
All Input and Output Voltage ^{1,2}	V _{IN} , V _{OUT}	-0.6	7.0	V
A9 Voltage ²	V _{ID}	-0.6	13.0	V
Weight			14.5	Grams
Thermal Impedance	Θ _{JC}	--	1.23	°C/W
Operating Temperature Range	T _{OPR}	-55	+125	°C
Storage Temperature Range	T _{STG}	-65	+150	°C

1. Relative to V_{SS}.

2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 20 ns.

TABLE 3. 27C1512T RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{CC}	4.5	5.5	V
Input Voltage	V _{IL} V _{IH}	-0.3 2.2	0.8 V _{CC} + 0.3	V
Operating Temperature Range	T _{OPR}	-55	+125	°C

TABLE 4. 27C1512T CAPACITANCE ^{1,2,3}

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}	--	10	pF
Output Capacitance	C_{OUT}	--	15	pF

1. $V_{IN} = V_{OUT} = 0V$.
2. $T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$.
3. Guaranteed by design.

TABLE 5. 27C1512T MODE SELECTION ^{1,2}

MODE	V_{PP}	V_{CC}	\overline{CE}	\overline{OE}	\overline{PGM}	A_9	I/O
READ	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
OUTPUT DISABLE	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
STANDBY	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
PROGRAM	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
PROGRAM VERIFY	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
PAGE DATA LATCH	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
PAGE PROGRAM	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
PROGRAM INHIBIT	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
IDENTIFIER	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H^2	ID

1. X = Don't care.
2. $11.5V \leq V_H \leq 12.5V$.

TABLE 6. 27C1512T DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

 $(V_{CC} = 5V \pm 10\%, V_{PP} = V_{SS}, T_A = -55 \text{ TO } +125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Input Leakage Current	$V_{IN} = 5.5V$ $V_{IN} @ 0V$	I_{LI}	1, 2, 3	--	--	2	μA
		I_{LI}		4	--	--	μA
Output Leakage Current High Low	$V_{OUT} = 5.5V$ $V_{OUT} = 0.45V$	I_{OH}	1, 2, 3	--	--	4	μA
		I_{OL}		-4.0	--	--	
Standby V_{CC} Current	$\overline{CE} = V_{IH}$	I_{SB}	1, 2, 3	--	--	2	mA
Operating V_{CC} Current	$I_{OUT} = 0 \text{ mA}, \overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}, f = 5 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}, f = 10 \text{ MHz}$	I_{CC1}	1, 2, 3	--	60	--	mA
		I_{CC2}		--	60	--	
		I_{CC3}		--	100	--	
V_{PP} Current	$V_{PP} = 5.5V$	I_{PP1}		--	1	40	μA
Input Voltage		V_{IH1}	1, 2, 3	2.2	--	--	V
		V_{IL1}		--	--	0.8	
Output Voltage	$I_{OH} = -800 \mu A$ $I_{OL} = 4.2 \text{ mA}$	V_{OH}	1, 2, 3	2.4	--	--	V
		V_{OL}		--	--	0.45	

TABLE 7. 27C1512T AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION ¹ $(V_{CC} = 5V \pm 10\%, V_{PP} = V_{SS}, T_A = -55 \text{ TO } +125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	t_{ACC}	9, 10, 11	--	200	ns
Chip Enable Access Time	$\overline{OE} = V_{IL}$	t_{CE}	9, 10, 11	--	200	ns
Output Enable Access Time	$\overline{CE} = V_{IL}$	t_{OE}	9, 10, 11	--	70	ns
Output Hold to Address Change	$\overline{CE} = \overline{OE} = V_{IL}$	t_{OH}	9, 10, 11	0	--	ns
Output Disable to High-Z ²	$\overline{CE} = V_{IL}$	t_{DF}	9, 10, 11	0	50	ns

1. Test conditions:

- Input pulse levels 0.45V/2.4V
- Input rise and fall times < 10 ns
- Output load 1 TTL gate + 100pF (including scope and jig)
- Referenced levels for measuring timing 0.8V/2.0V

2. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.TABLE 8. 27C1512T DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS ^{1,2,3,4} $(V_{CC} = 6.25V \pm 0.25V, V_{PP} = 12.5V \pm 0.3V, T_A = 25^\circ\text{C} \pm 5^\circ\text{C})$

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUP	MIN	MAX	UNIT
Input Leakage Current	$V_{IN} = 0V \text{ TO } V_{CC}$	I_{LI}	1	--	2	μA

TABLE 8. 27C1512T DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS ^{1,2,3,4}
 $(V_{CC} = 6.25V \pm 0.25V, V_{PP} = 12.5V \pm 0.3V, T_A = 25^\circ C \pm 5^\circ C)$

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUP	MIN	MAX	UNIT
Operating V_{CC} Current		I_{CC}	1	--	30	mA
Operating V_{PP} Current	$\overline{CE} = \overline{PGM} = V_{IL}$	I_{PP}	1	--	80	mA
Input Voltage ⁵		V_{IH}	1	2.2	--	V
		V_{IL}	1	--	0.8	
Output Voltage	$I_{OH} = -400 \mu A$	V_{OH}	1	2.4	--	V
	$I_{OH} = 2.1 mA$	V_{OL}	1	--	0.45	

1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
2. V_{PP} must not exceed 13V, including overshoot.
3. Do not change V_{PP} from V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE} = \text{low}$.
4. DC electrical parameters for programming operations are not tested. These parameters are guaranteed by design.
5. Device reliability may be adversely be affected if the device is installed or removed while $V_{PP} = 12.5V$.

TABLE 9. 27C1512T AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS ^{1,2}
 $(V_{CC} = 6.25V \pm 0.25V, V_{PP} = 12.5V \pm 0.3V, T_A = -55 \text{ TO } +125^\circ C)$

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Address Setup Time	t_{AS}	9, 10, 11	2	--	μs
Address Hold Time	t_{AH}	9, 10, 11	0	--	μs
Data Setup Time	t_{DS}	9, 10, 11	2	--	μs
Data Hold Time	t_{DH}	9, 10, 11	2	--	μs
Chip Enable Setup Time	t_{CES}	9, 10, 11	2	--	μs
V_{PP} Setup Time	t_{VPS}	9, 10, 11	2	--	μs
V_{CC} Setup Time	t_{VCS}	9, 10, 11	2	--	μs
Output Enable Setup Time	t_{OES}	9, 10, 11	2	--	μs
Output Disable Time	t_{DF}^3	9, 10, 11	0	130	ns
PGM Initial Programming Pulse Width	t_{PW}	9, 10, 11	0.19	0.21	ms
PGM Overprogramming Pulse Width	t_{OPW}	9, 10, 11	0.19	5.25	ms
Data Valid from Output Enable Time	t_{OE}	9, 10, 11	0	150	ns
Output Enable Pulse During Data Latch	t_{LW}	9, 10, 11	1	--	μs
Output Enable Hold Time	t_{OEH}	9, 10, 11	2	--	μs
Chip Enable Hold Time	t_{CEH}	9, 10, 11	2	--	μs
PGM Setup Time	t_{PGMS}	9, 10, 11	2	--	μs

1. Test conditions:
 - Input pulse levels 0.45V
 - Input rise and fall times ≤ 20 ns
 - Referenced levels for measuring timing 0.8V/2.0V
2. AC electrical parameters for programming operations are not tested. These parameters are guaranteed by design.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

FIGURE 1. READ TIMING WAVEFORM

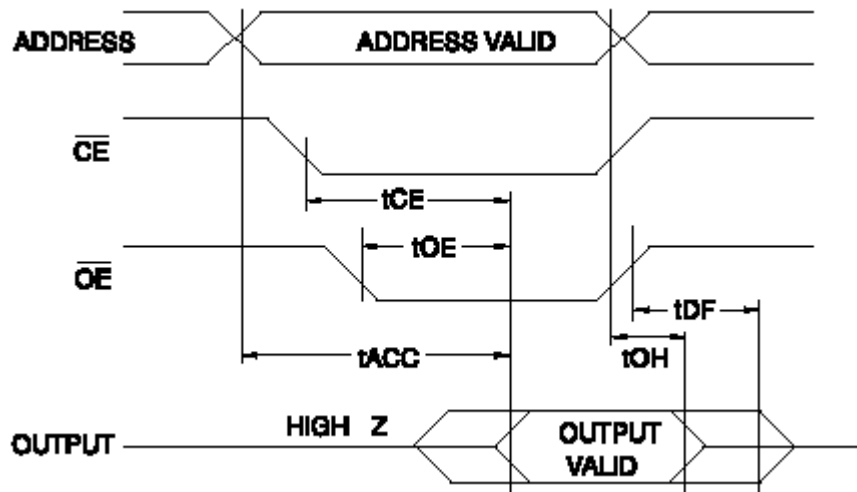


FIGURE 2. BYTE PROGRAMMING FLOWCHART

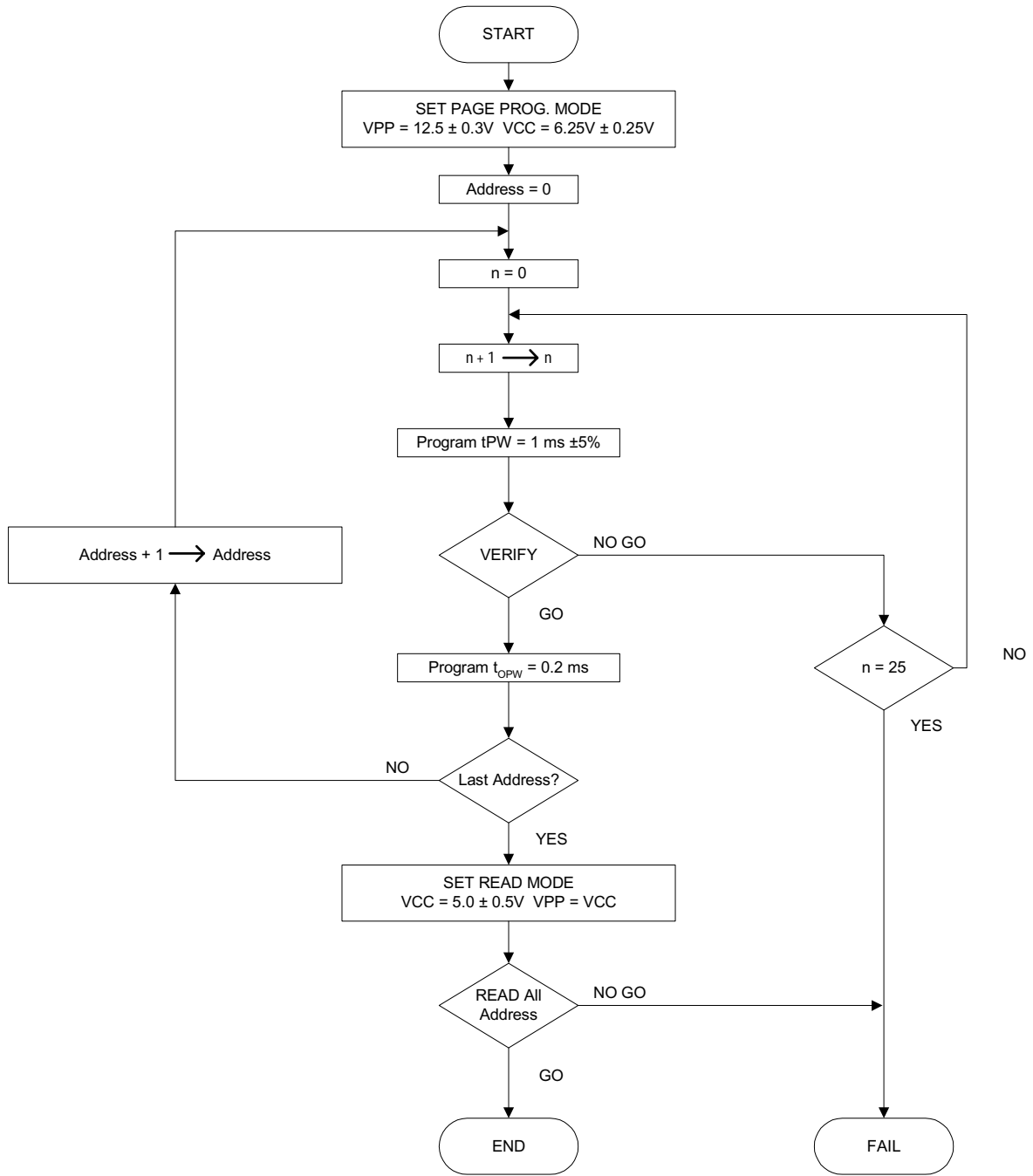


FIGURE 3. BYTE PROGRAMMING TIMING WAVEFORM

■ BYTE PROGRAMMING TIMING WAVEFORM

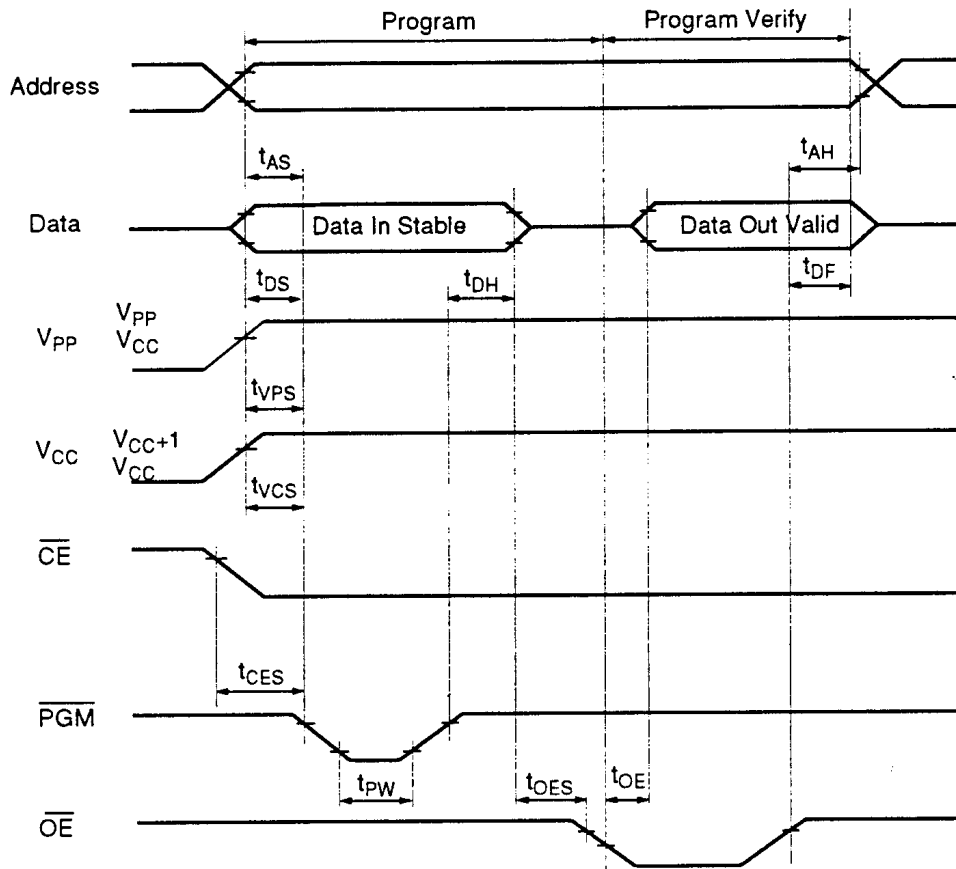


FIGURE 4. PAGE PROGRAMMING FLOWCHART

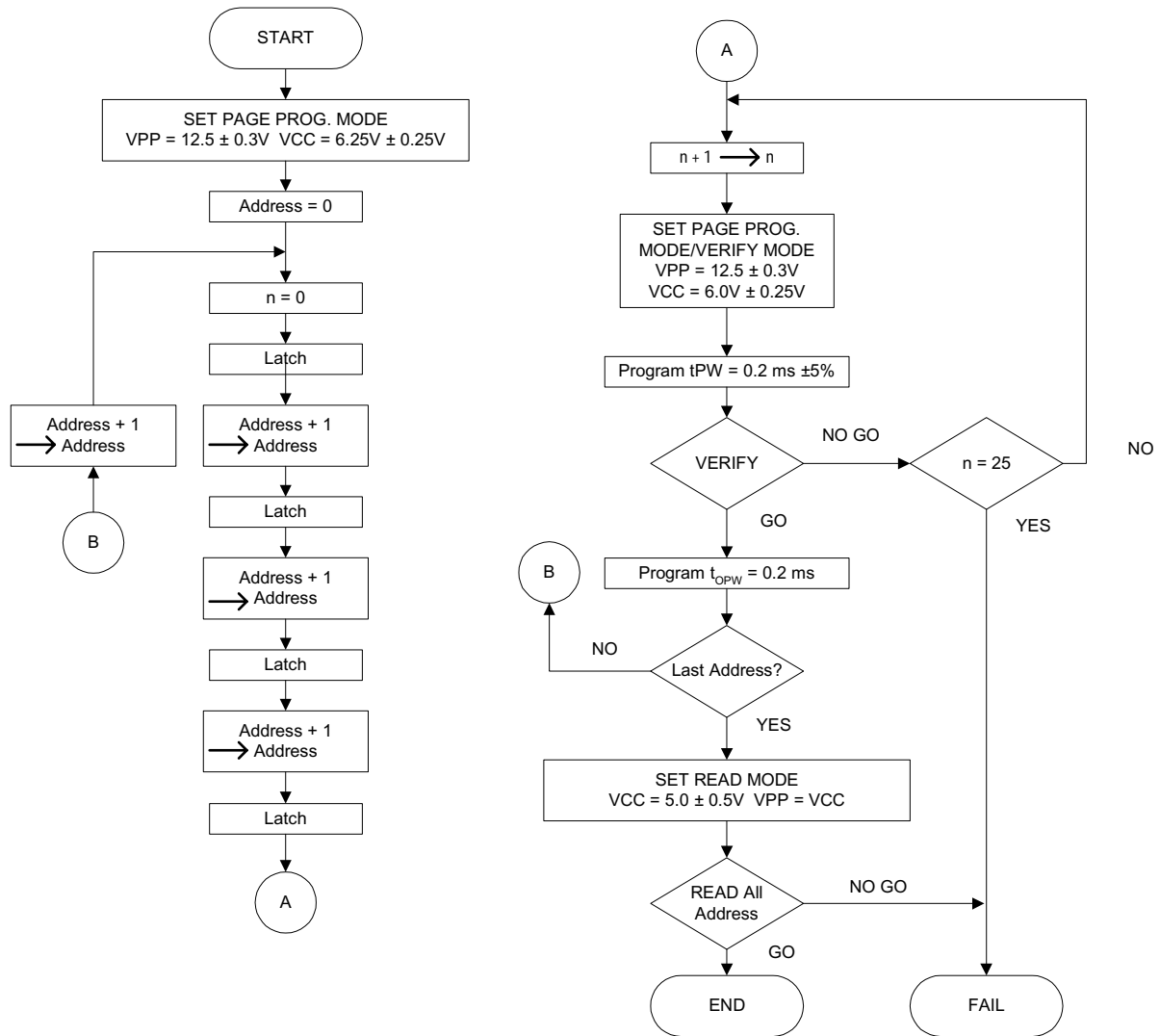
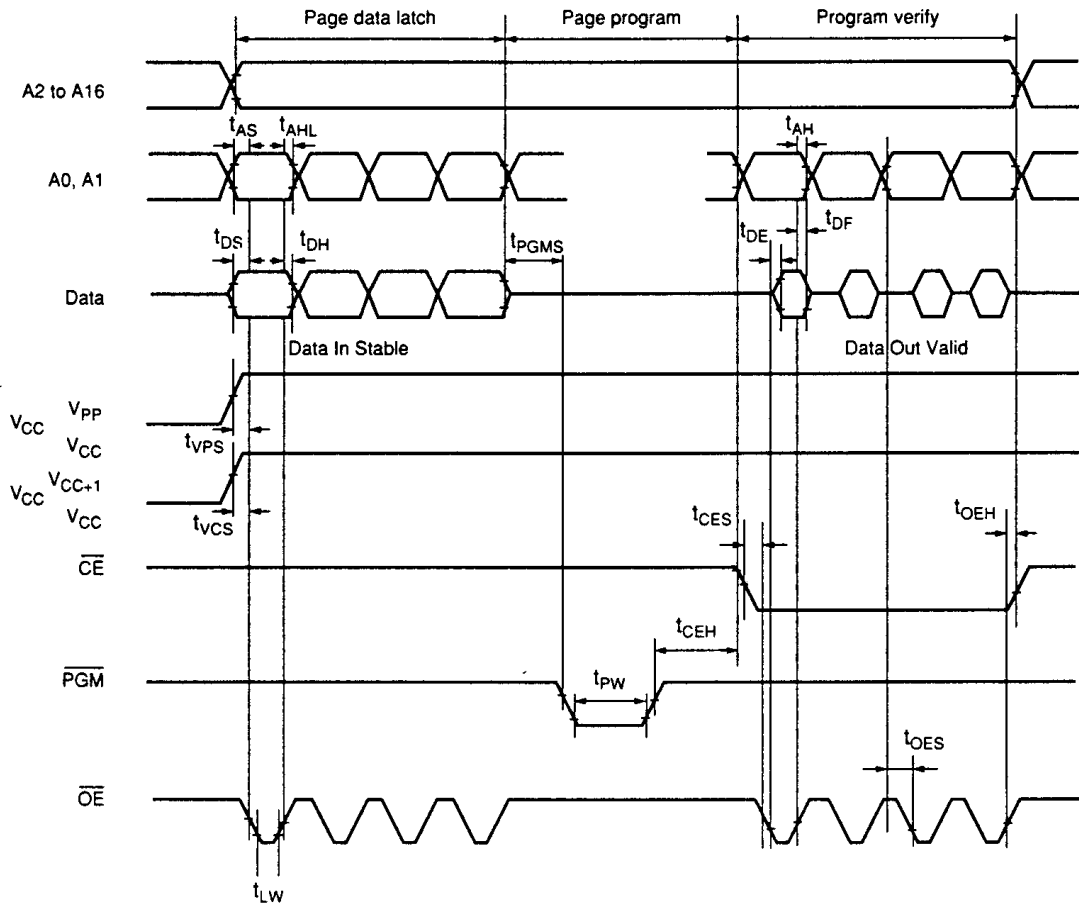
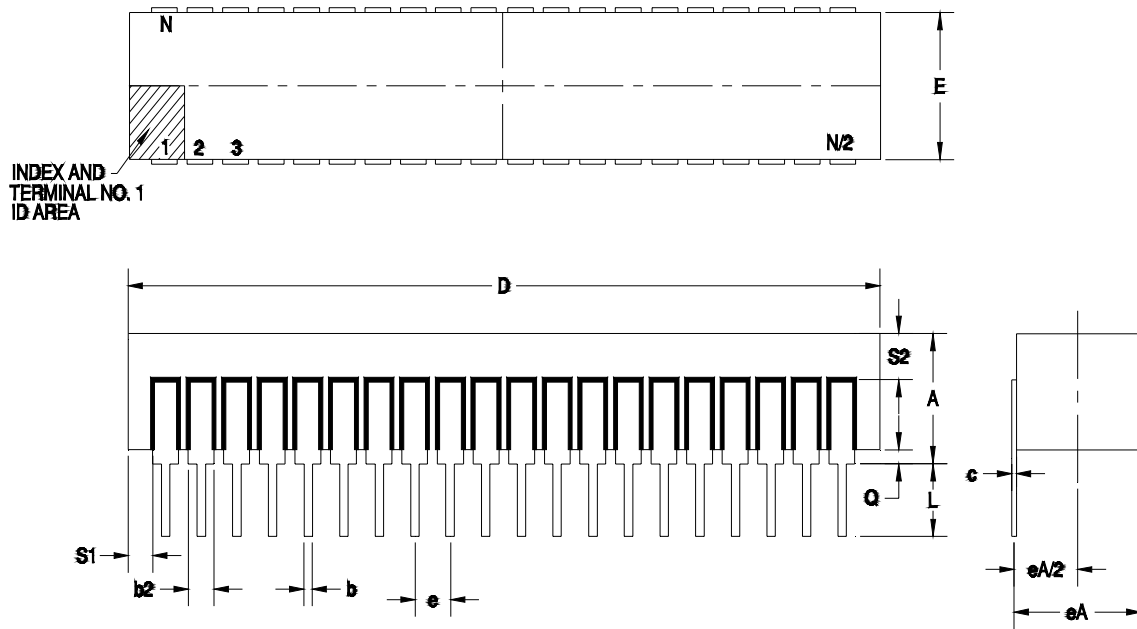


FIGURE 5. PAGE PROGRAMMING TIMING WAVEFORM





40 PIN RAD-PAK® DIP

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.152	0.225
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.012
D	--	2.000	2.096
E	0.510	0.595	0.620
e	0.100 BSC		
eA	0.600 BSC		
eA/2	0.300 BSC		
L	0.140	0.150	0.160
Q	0.015	0.050	0.070
S1	0.005	0.025	--
S2	0.005	--	--
N	40		

Note: All dimensions in inches

Because of package size, constant acceleration is less than 3,000 g's.

Important Notice:

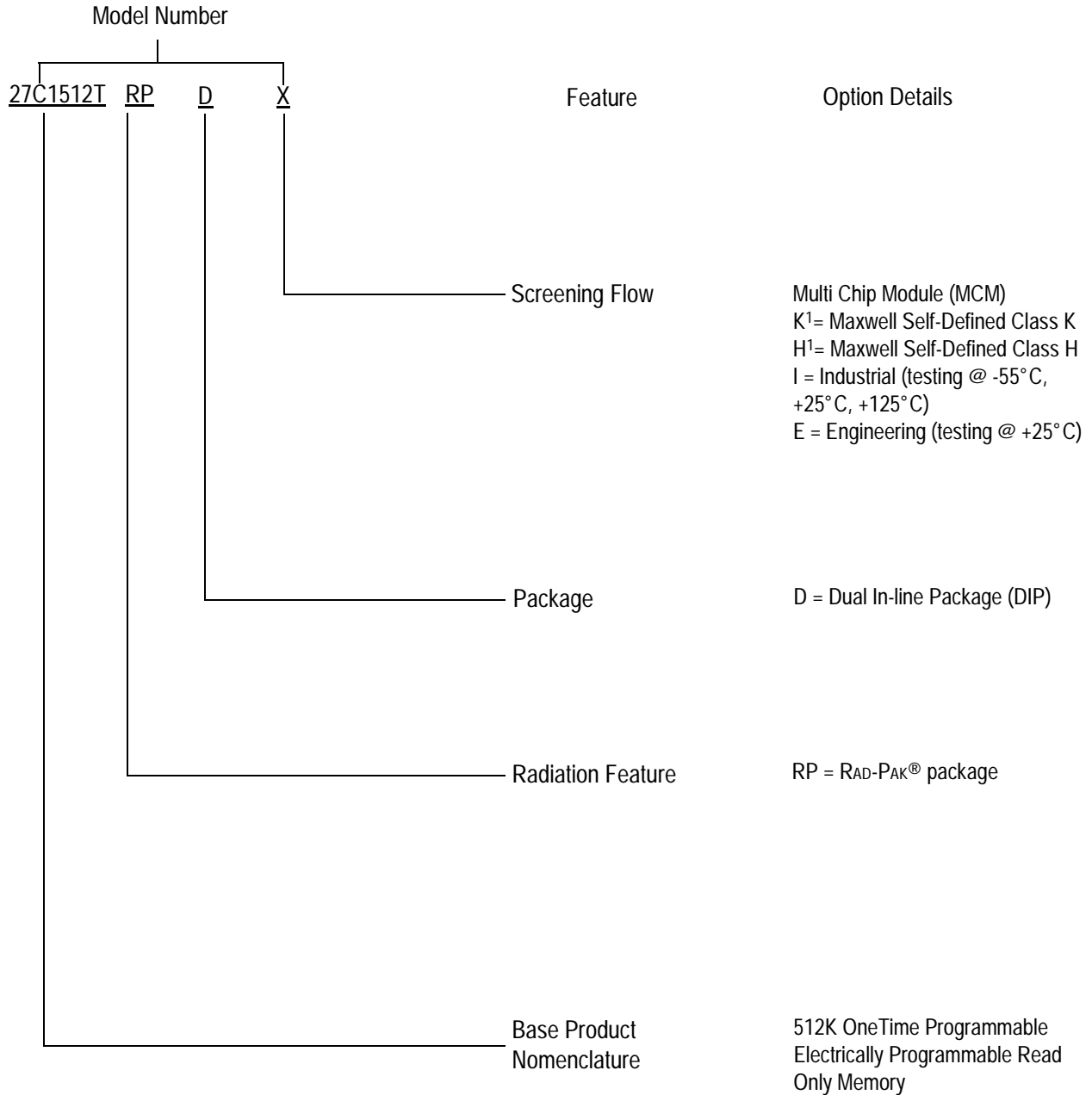
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Product Ordering Options



1) Products are manufactured and screened to Maxwell Technologies self-defined Class Hand Class K flows.