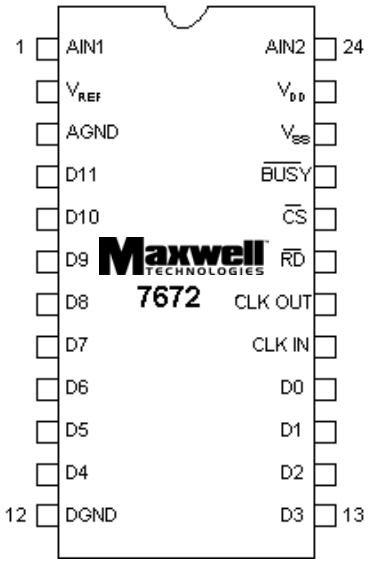
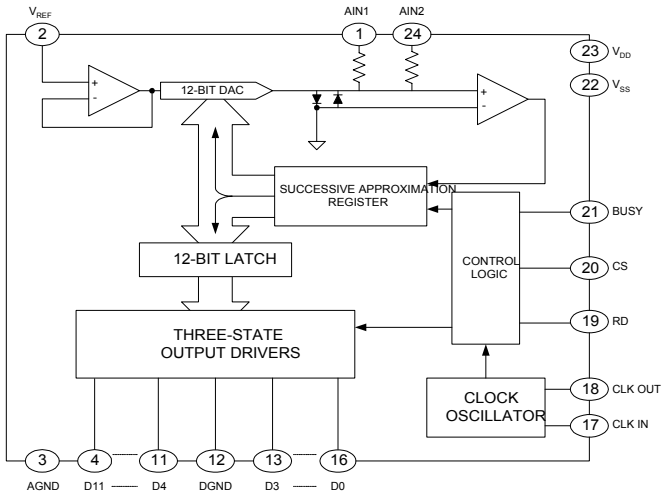
7672
12-Bit A/D Converter





Logic Diagram

FEATURES:

- 12-bit high speed A/D converter
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effect
  - SEL > 120 Mev/mg/cm^2
  - SEU_{TH} > 5.8 Mev/mg/cm^2
  - SEU_{Sat} = -1E-4 cm^2/Device
- Package:
  - 24 pin RAD-PAK® flat package
  - 24 pin RAD-PAK® DIP
- Fast conversion times:
  - 7672-05: 5 µs
- Low 110 mW typical power consumption
  - Corrects all single-bit errors
  - Detects all double and some triple-bit errors
- High-speed BiCMOS technology
  - Choice of +5V and +10V input ranges
  - Operates with +5V and -12V power supplies
  - Fast 125 ns bus-access time

DESCRIPTION:

Maxwell Technologies' 7672 high-speed 12-bit analog-to-digital converter microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 7672 uses an accurate high-speed DAC and comparator to achieve conversion time as low as 5 µs while dissipating only 110 mW of power. The 7672 is designed to be used with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive multiple 7672s from a single system reference, since the reference input is buffered and draws very little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low cost reference can be used. For optimal precision, a high accuracy reference where an absolute 12-bit accuracy can be obtained over a wide temperature range may be used. Analog input range is pin-selectable for 0 to +5V, 0 to +10V, or ±5V, making the ADC ideal for data acquisition and analog input/output cards. A high-speed digital interface (125 ns data access time) with three state data outputs is compatible with most microprocessors.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 7672 PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	AIN1	Analog Input
2	V_{REF}	Voltage-Reference Input
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3-D0	Three-State Data Outputs
17	CLKIN	Clock Input
18	CLKOUT	Clock Output
19	$\overline{RD}$	READ Input
20	$\overline{CS}$	CHIP SELECT
21	$\overline{BUSY}$	BUSY
22	V_{SS}	Negative Supply, -12V
23	V_{DD}	Positive Supply, +5V
24	AIN2	Analog Input

TABLE 2. 7672 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage to DGND	V_{DD}	-0.3	7.0	V
Negative Supply Voltage to DGND	V_{SS}	-17	+0.3c	V
AGND to DGND	--	-0.3	V_{DD} +0.3	V
AIN1, AIN2 to AGND	--	-15	+15	V
Digital Input Voltage to DGND	V_{IN}	-0.3	V_{DD} +0.3	V
Digital Output Voltage to DGND	V_{OUT}	-0.3	V_{DD} +0.3	V
V_{REF} to AGND	--	V_{SS} -0.3	V_{DD} +0.3	V
Power Dissipation to +75°C	P_D	--	1000	mW
Power Dissipation above 75°C (Derate)	--	--	10	mW/°C
Thermal Impedance	Θ_{JC}	--	3.24	°C/W
Storage Temperature Range	T_{STG}	-65	+150	°C
Operating Temperature Range	T_A	-55	+125	°C

TABLE 3. 7672 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	1	V_{DD}	4.75	5.25	V
Negative Supply Voltage	1	V_{SS}	-13.2	-10.8	V
V_{REF} Input Range	1	V_{REF}	-5.05	-4.95	V
Power Dissipation V_{DD} = 5V, V_{SS} = -12V	1	P_D	--	179	mW

TABLE 4. 7672 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = -12V ±10%, V_{REF} = -5V, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	SUBGROUPS	MIN	MAX	UNITS
Input Low Voltage	V_{IL}		1, 2, 3	--	0.8	V
Input High Voltage	V_{IH}		1, 2, 3	2.4	--	V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA	1, 2, 3	--	0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = -200 µA	1, 2, 3	4.0	--	V
Input Leakage Current	I_{IN}	($\overline{CS}$,$\overline{RD}$) V_{IN} = V_{DD} or GND (CLKIN) V_{IN} = V_{DD} or GND	1, 2, 3	-- --	±10 ±20	µA
Output Leakage Current	I_{LKG}	(D0-D11) V_{OUT} = V_{DD} or GND	1, 2, 3	--	±10	µA
Input Capacitance [1]	C_{IN}			--	10	pF
Floating State Output Capacitance[2]	C_{OUT}			--	15	pF
Power Supply Current	I_{DD} I_{SS}		1, 2, 3	-- --	7 -12	mA
Power Supply Rejection, V_{DD}	PSRR (V_{DD})	V_{DD} = 4.75 to 5.25 volts V_{SS} = -12V	1, 2, 3	--	±1	LSB
Power Supply Rejection, V_{SS}	PSRR (V_{SS})	V_{SS} = -10.8 to -13.2 volts V_{DD} = 5V	1, 2, 3	--	±1	LSB
Analog Input Current (AIN1 or AIN2)	I_{AIN}	Unipolar Range: 0 to 5 V, 10V Bipolar Range: ±5V	1, 2, 3	-- --	±3.5 ±1.75	mA
V_{REF} Input Range [1]	V_{REF}		1, 2, 3	-5.05	-4.95	V
V_{REF} Input Current	I_{REF}		1, 2, 3	--	±3	µA
Resolution	RES	T_A = -55 to +125°C	1, 2, 3	12	--	bits
Integral Nonlinearity	INL	T_A = +25 °C T_A = -55 to +125°C	1 2, 3	-- --	±1 ±1	LSB
Differential Nonlinearity	DNL	12 bits, no missing codes T_A = -55 to +125˚C	1, 2, 3	--	±0.9	LSB
Unipolar Offset Error	UOE	T_A = +25˚C T_A = -55 to +125˚C	1 2, 3	-- --	±5 ±6	LSB
Unipolar Gain Error	UGE	T_A = +25 ˚C T_A = -55 to +125˚C	1 2, 3	-- --	±5 ±7	LSB

TABLE 4. 7672 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = -12V ±10%, V_{REF} = -5V, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	SUBGROUPS	MIN	MAX	UNITS
Bipolar Zero Error	BZE	T_A = +25˚C T_A = -55 to +125˚C	1 2, 3	-- --	±5 ±6	LSB
Bipolar Gain Error	BGE	T_A = +25˚C T_A = -55 to +125˚C	1 2, 3	-- --	±5 ±7	LSB

1. Guaranteed by design.

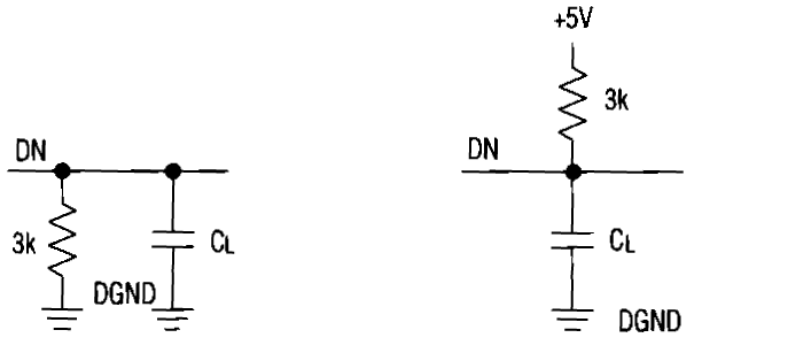
TABLE 5. 7672 TIMING CHARACTERISTICS [1,2]

(V_{DD} = 5V ±5%, V_{SS} = -12V ±10%, V_{REF} = -5V, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITION	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Conversion Time, Synchronous Clk, [3]	12.5 clks, TA = -55 to +125 °C	9, 10, 11	tCONV	--	5.0	us
Conversion Time, Asynchronous Clk,	12-13 clks, TA = -55 to +125 °C	9, 10, 11	tCONV	4.8	5.2	us
CS to RD Setup Time	TA = -55 to +125 °C	9, 10, 11	t1	0	--	ns
RD to BUSY Delay	CL = 50 pF, TA = +25 °C CL = 50 pF, TA = -55 to +125 °C	9 10, 11	t2	-- --	190 270	ns
Data Access Time [4]	CL = 100 pF, TA = +25 °C CL = 100 pF, TA = -55 to +125 °C	9 10, 11	t3	-- --	125 170	ns
RD Pulse Width	TA = -55 to +125 °C	9, 10, 11	t4	t3	--	ns
CS to RD Hold Time	TA = -55 to +125 °C	9, 10, 11	t5	0	--	ns
Data Setup Time After BUSY4	CL = 100 pF, TA = +25 °C CL = 100 pF, TA = -55 to +125 °C	9 10, 11	t6 --	-- --	70 100	ns
Bus Relinguish Time[5]	(TA = +25 °C) (-55 < TA < +125 °C)	9 10, 11	t7	-- --	75 90	ns
Delay Between Read Operations	(-55 < TA < +125 °C)	9, 10, 11	t8	200	--	ns

1. 1LSB = FS/4096; T_A = 25 ˚C; Performance over power supply tolerance is guaranteed by power supply rejection test.
2. All inputs are 0V to +5V swing with $t_r = t_r$ = 5ns (10 to 90% of +5V) and timed from a voltage level of +1.6V.
3. Functionally tested.
4. t3 and t6 are measured with the load circuits of Figure 1 and are defined as the time required for an output to cross +0.8 or +2.4.
5. t7 is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 2.

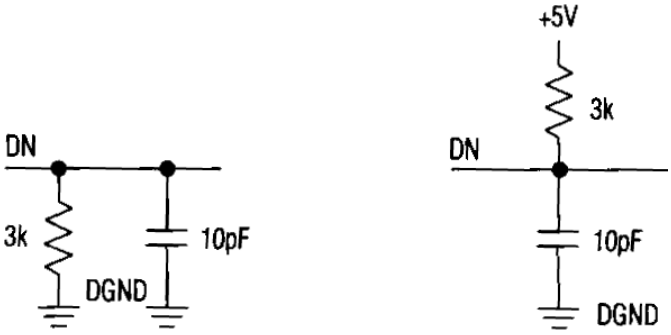
FIGURE 1. LOAD CIRCUITS FOR ACCESS TIME



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

FIGURE 2. LOAD CIRCUIT FOR BUS RELINQUISH TIME



a. V_{OH} to High-Z

b. V_{OL} to High-Z

FIGURE 3.

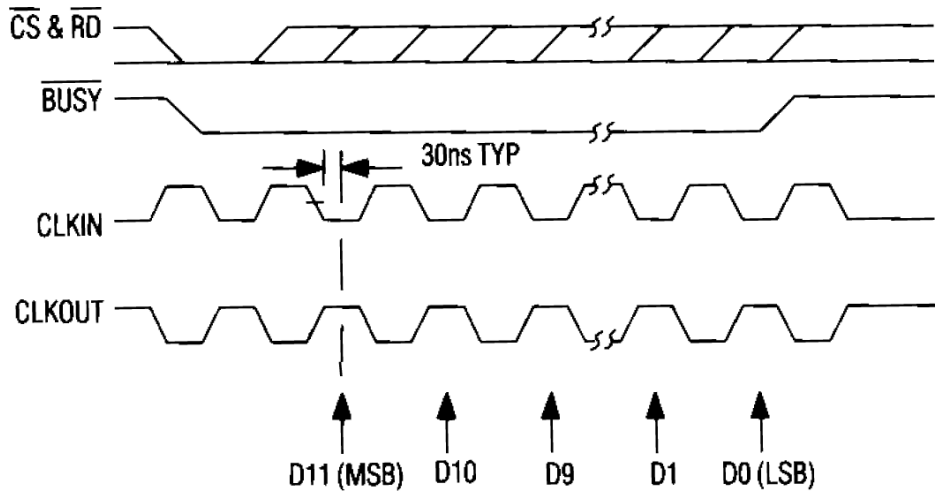
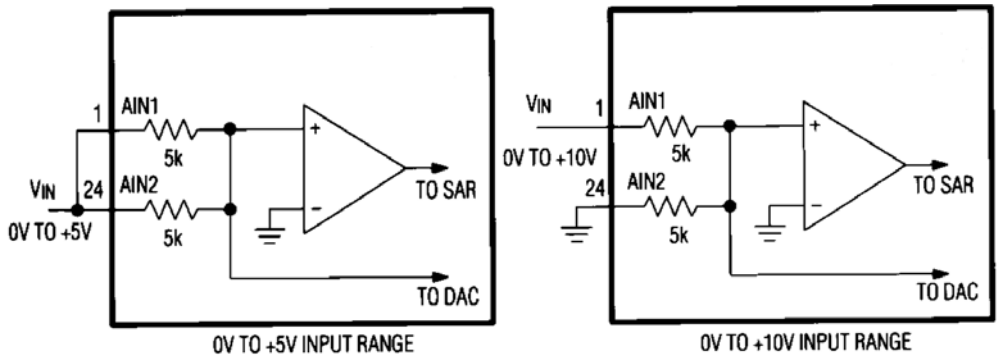
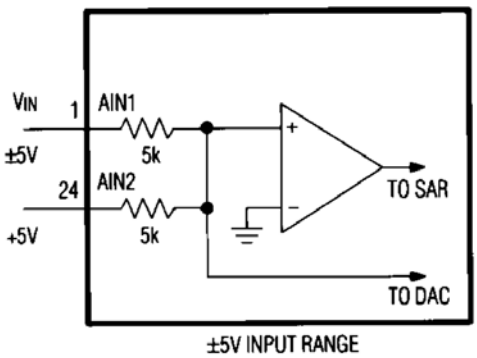


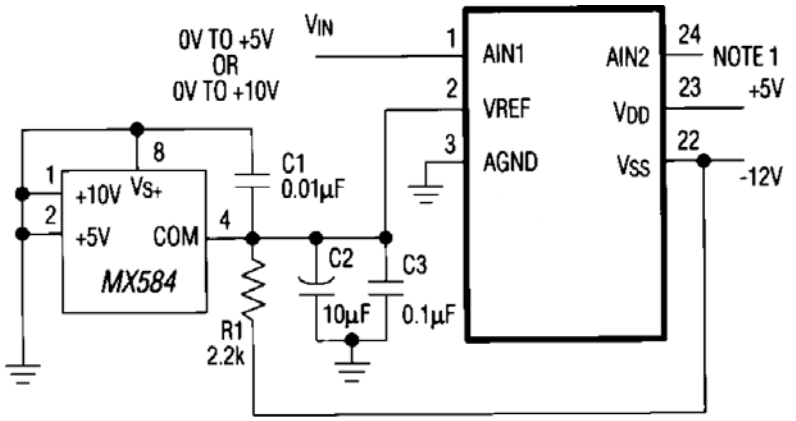
FIGURE 4. ANALOG INPUT RANGE CONFIGURATIONS



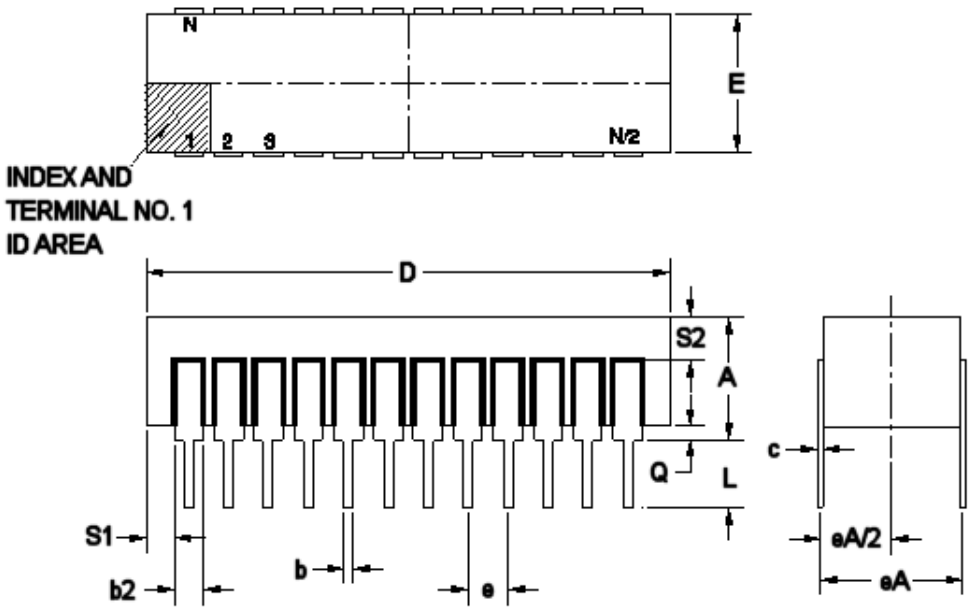


(CONFIGURATIONS ARE 24-PIN DIP)

FIGURE 5. UNIPOLAR OPERATING USING A REFERENCE



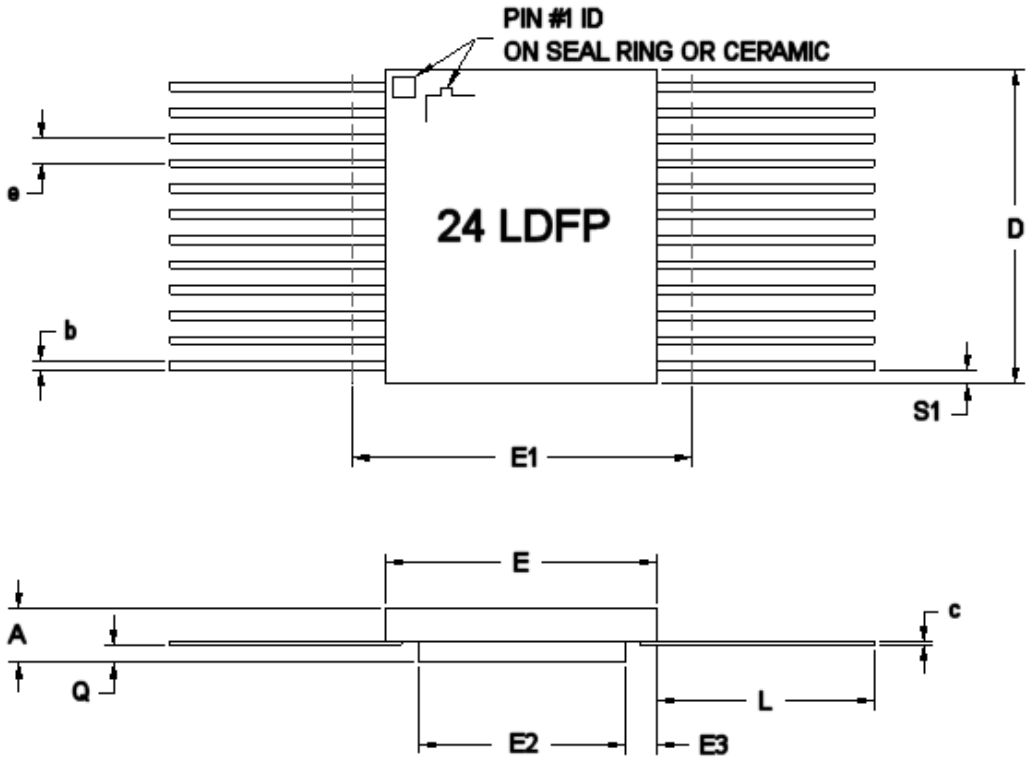
(CONFIGURATION IS 24-PIN DIP)



24 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.167	0.200
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.200	1.280
E	0.510	0.594	0.620
eA	0.600 BSC		
eA/2	0.300 BSC		
e	0.100 BSC		
L	0.135	0.145	0.155
Q	0.015	0.030	0.045
S1	0.005	0.025	--
S2	0.005	--	--
N	24		

D24-02
Note: All dimensions in inches



24 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.153	0.170	0.183
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.596	0.640
E	0.350	0.400	0.420
E1	--	--	0.450
E2	0.180	0.236	--
E3	0.030	0.082	--
e	0.050 BSC		
L	0.315	0.325	0.335
Q	0.026	0.050	0.056
S1	0.005	0.015	--
N	24		

F24-01
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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