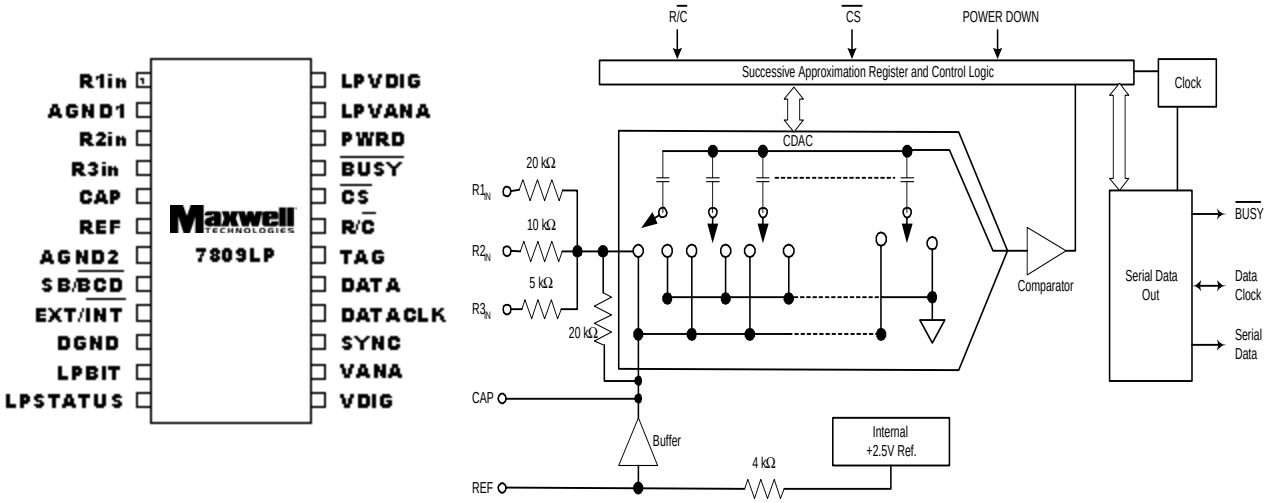
7809LP
16-Bit Latchup Protected Analog to Digital Converter



Logic Diagram

FEATURES:

- RAD-PAK® radiation-hardened against natural
- space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Latch-up Protection Technology (LPT™)
- SEL converted into a reset
  - Rate based on cross section and mission
- Package: 24 pin RAD-PAK flat package
- 100 kHz min sampling rate
- ±10 V and 0 V to 5 V input range
- DNL: 15-bits "No Missing Codes"
- 83 dB min SINAD with 20 kHz input
- Single +5 V supply operation
- Utilizes internal or external reference
- Serial output
- Power dissipation: 132 mW max

DESCRIPTION:

Maxwell Technologies' 7809LP high-speed 16-bit analog to digital converter features a greater than 100 kilorad (Si) total dose tolerance depending upon space mission. Using Maxwell's radiation-hardened RAD-PAK® packaging technology is latchup protected by Maxwell Technologies' Latchup Protection Technology (LPT™). It is a 24 pin, 16-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. The 7809LP contains a 16-bit capacitor based SAR A/D with S/H, reference, clock, interface for microprocessor use, and serial output drivers. The 7809LP is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges include ±10 V and 0 to 5 V, while the innovative design allows operation from a single +5 V supply, with power dissipation of under 132 mW.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 50 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defined Class K.

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TABLE 1. 7809LP PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	R1IN	Analog Input.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	R2IN	Analog Input.
4	R3IN	Analog Input.
5	CAP	Reference Buffer Capacitor. 2.2 µF tantalum to ground.
6	REF	Reference Input/Output. 2.2 µF tantalum capacitor to ground.
7	AGND2	Analog Ground.
8	SB/$\overline{\text{BTC}}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/INT	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	LPBIT	Built In test function of the latchup protection. Drive LOW during normal operation.
12	LPSTATUS	Latchup Protection Status Output. LPSTATUS when HIGH indicates latchup protection is active and output data is invalid.
13	VDIG	Digital Supply Input. Nominally 5V.
14	VANA	Analog Supply Input. Nominally 5V.
15	SYNC	Sync Output. If EXT/INT is HIGH, either a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW or a falling edge on $\overline{\text{CS}}$ with R/$\overline{\text{C}}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
16	DATACLK	Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
17	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16-bits of data, the 7809LOPO will output the level input of TAG as long as $\overline{\text{CS}}$ is LOW and R/$\overline{\text{C}}$ is HIGH. If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
18	TAG	Tag input for use in external clock mode. If EXT/INT is HIGH, the digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{\text{CS}}$ is LOW and R/$\overline{\text{C}}$ is HIGH.
19	R/$\overline{\text{C}}$	Read/Convert Input. With $\overline{\text{CS}}$ LOW, a falling edge on R/$\overline{\text{C}}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW, or a falling edge on $\overline{\text{CS}}$ with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
20	$\overline{\text{CS}}$	Chip Select. Internally OR'ed with R/$\overline{\text{C}}$.

Table 1. 7809LP Pin Description

Pin	Symbol	Description
21	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
22	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversions are maintained in the output shift register.
23	LPVANA	Latchup Protection Analog Supply.
24	LPVDIG	Latchup Protection Digital Supply.

Table 2. 7809LP Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Inputs	$R1_{IN}$ $R2_{IN}$ $R3_{IN}$ CAP REF [1]	-25 -25 -25 V_{ANA} + 0.3	25 25 25 AGND2 - 0.3	V V V V
Ground Voltage Differences: DGND, AGND2		-0.3	0.3	V
V_{ANA}		--	7	V
V_{DIG}			7	V
V_{DIG} to V_{ANA}		--	0.3	V
Specified Performance		-40	85	˚C
Digital Inputs		-0.3	V_{DIG} + 0.3	V
Storage Temperature	T_{STG}	-65	150	˚C

1. Indefinite short to AGND2, momentarily short to V_{ANA}.

Table 3. 7809LP DC Accuracy Specifications

(Specified Performance -40 to +85°C)

Parameter	Subgroups	Min	Typ	Max	Unit
Integral Linearity Error -40 to 85°C	1 2, 3	-- --	-- --	±3 ±5	LSB [1]
Differential Linearity Error -40 to 85°C	1 2, 3	-- --	-- --	-2, 3 -1, 6	LSB LSB
No Missing Codes [2]		15	--	--	Bits
Transition Noise [3]		--	1.3	--	LSB
Full Scale Error [4,5]	1, 2, 3	--	--	±0.6	%
Full Scale Error [4,5] (using ext. 2.5000 V_{ref})	1, 2, 3	--		±0.6	%
Full Scale Error Drift	--	--	±7	--	ppm/˚C

TABLE 3. 7809LP DC ACCURACY SPECIFICATIONS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Full Scale Error Drift (using ext. 2.5000 V_{ref})	1, 2, 3	--	±2	--	ppm/°C
Bipolar Zero Error [4]	1, 2, 3	--	--	±10	mV
Bipolar Zero Error Drift		--	±2	--	ppm/°C
Unipolar Zero Error [4] -40 to 85°C	1 2, 3	-- --	-- --	±3 ±16	mV mV
Unipolar Zero Error Drift		--	±2	--	ppm/°C
Recovery to Rated Accuracy after Power Down (1 uF Capacitor to CAP)		--	1	--	ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$) 4.75 V ≤ V_D ≤ 5.2 V -40 to 85°C	1 2, 3	-- --	-- --	±8 ±32	LSB LSB

1. LSB stands for Least Significant Bit. One LSB is equal to 305 µV.
2. Not tested.
3. Typical rms noise at worst case transitions and temperatures.
4. Measured with various fixed resistors.
5. For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last scale code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

TABLE 4. DELTA LIMITS

PARAMETER	VARIATION
I_{CC}	+/- 10%

Parameters are measured and recorded asDeltas per MIL-STD-883, as specified in Table 11.

TABLE 5. 7809LP DIGITAL INPUTS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
V_{IL}	1, 2, 3	-0.3	--	0.8	V
V_{IH}		2.0	--	V_D + 0.3	V
I_{IL}, I_{IH}		--	--	±10	µA

TABLE 6. 7809LP ANALOG INPUT AND THROUGHPUT SPEED

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Voltage Ranges	1, 2, 3	10 V, 0 V to 5 V See Table 2.			
Impedance	1, 2, 3				
Capacitance[1]		--	35	--	pF
Conversion Time	9, 10, 11	--	7.6	8	µs
Complete Cycle (Acquire and Convert)	9, 10, 11	--	--	10	µs
Throughput Rate [2]	9, 10, 11	100	--	--	kHz

1. Guarenteed by design.
2. Tested by application of signal.

TABLE 7. 7809LP AC ACCURACY SPECIFICATIONS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, f_{IN} = 20 kHz [1]	4, 5, 6	90	100	--	dB [2]
Total Harmonic Distortion, f_{IN} = 20 kHz [1]	4, 5, 6	--	-100	-90	dB
Signal-to-Noise (Noise + Distortion) [1] f_{IN} = 20 kHz -60 dB Input	4, 5, 6	 83 --	 88 30	 -- --	dB
Signal-to-Noise [1], f_{IN} = 20 kHz		83	88	--	dB
Full-Power Bandwidth [1,3]		--	250	--	kHz

1. Guaranteed by design.
2. All specifications in dB are referred to a full-scale ±10 V input.
3. Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-Noise (Noise + Distortion) degrades to 60 dB.

TABLE 8. 7809LP SAMPLING DYNAMICS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Aperture Delay		--	40	--	ns
Aperture Jitter	9, 10, 11	Sufficient to meet AC specification			
Transient Response FS Step		--	2	--	us
Overvoltage Recovery [1]		--	150	--	ns

1. Recovers to specified performance after 2 X FS input overvoltage.

TABLE 9. 7809LP REFERENCE

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must be ext. buffer)		--	1	--	µA
External Reference Voltage Range for Specified Linearity [1]		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref	--	--	100	µA

1. Tested by application of signal.

TABLE 10. 7809LP DIGITAL OUTPUTS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
Data Format Data Coding Pipeline Delay		Serial 16-bits Binary Two's Complement or Straight Binary Conversion results only available after completed conversion				
Data Clock	Selectable for internal or external data clock					
Internal (Output Only When Transmitting Data) External (Can Run Continually)	9, 10, 11	EXT/$\overline{INT}$ Low EXT/$\overline{INT}$ High	-- 0.1	2.3 --	-- 10	MHz
V_{OL} V_{OH}	1, 2, 3	I_{SINK} = 1.6 mA I_{SOURCE} = 500 µA	-- 4	-- --	0.4 --	V
Leakage Current [1]		High-Z State, V_{OUT} = 0V to V_{DIG}	--	--	±10	µA
Output Capacitance [1]		High-Z State	--	15	--	pF

1. Not tested.

TABLE 11. 7809LP POWER SUPPLIES

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG}	1, 2, 3	Must be < V_{ANA}	4.75	5	5.25	V
V_{ANA}	1, 2, 3		4.75	5	5.25	V
I_{DIG}			--	0.3	--	mA
I_{ANA}			--	16	--	mA
Icc	1, 2, 3	IDIG +IANA @ 100KHz			26.4	mA

TABLE 11. 7809LP POWER SUPPLIES

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation	1, 2, 3					mW
PWRD LOW		$V_{ANA} = V_{DIG} = 5V$	--	--	132	
PWRD HIGH[1]		f_s = 100 kHz	--	--	100	

1) Not Tested

TABLE 12. 7809LP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data using Internal Clock	1 > 0	0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n-1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK
	0	1 > 0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n-1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK
Initiate Conversion and Output Data using External Clock	1 > 0	0	1	1	Input	0	x	Initiates conversion “n”
	0	1 > 0	1	1	Input	0	x	Initiates conversion “n”
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion “n” clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pules on SYNC followed by data from conversion “n-1” clocked out synchronized to external DATACLK [1]. Conversion “n” in process.
	0	0 > 1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion “n-1” clocked out synchronized to external DATACLK [1]. Conversion “n” in process.
Incorrect Conversions	0	0	0 > 1	x	x	0	x	CS or R/C must be HIGH or a new conversion will be initiated without time for acquisition

TABLE 12. 7809LP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion will be initiated without time for acquisition
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

1. See Figure 4 for constraints on previous data valid during conversion.

TABLE 13. 7809LP INPUT RANGE CONNECTION

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9 kΩ
±5V	AGND	V_{IN}	CAP	13.3 kΩ
±3.3V	V_{IN}	V_{IN}	CAP	10.7 kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0 kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7 kΩ

TABLE 14. 7809LP CONVERSION AND DATA TIMING

(T_A = -40 °C TO 85 °C UNLESS OTHERWISE SPECIFIED)

SYMBOL	DESCRIPTION	SUBGROUPS	MIN	TYP	MAX	UNIT
t1	Convert Pulse Width	9, 10, 11	40	--	6000	ns
t2	$\overline{BUSY}$ Delay	9, 10, 11	--	--	65	ns
t3	$\overline{BUSY}$ LOW	9, 10, 11	--	--	8	µs
t4	$\overline{BUSY}$ Delay after End of Conversion	9, 10, 11	--	220	--	ns
t5	Aperture Delay	9, 10, 11	--	40	--	ns
t6	Conversion Time	9, 10, 11	--	7.6	8	µs
t7	Acquisition Time	9, 10, 11	--	--	2	µs
t6 + t7	Throughput Time	9, 10, 11	--	9	10	µs

Table 14. 7809LP Conversion and Data Timing

(T_A = -40 °C to 85 °C unless otherwise specified)

Symbol	Description	Subgroups	Min	Typ	Max	Unit
t8	R/$\overline{C}$ Low to DATACLK Delay	9, 10, 11	--	450	--	ns
t9	DATACLK Period	9, 10, 11	--	440	--	ns
t10	Data Valid to DATACLK HIGH Delay	9, 10, 11	20	75	--	ns
t11	Data Valid after DATACLK LOW Delay	9, 10, 11	100	125	--	ns
t12	External DATACLK	9, 10, 11	100	--	--	ns
t13	External DATACLK HIGH	9, 10, 11	20	--	--	ns
t14	External DATACLK LOW	9, 10, 11	30	--	--	ns
t15	DATACLK HIGH Setup Time	9, 10, 11	20	--	t12 + 5	ns
t16	R/$\overline{C}$ to $\overline{CS}$ Setup Time	9, 10, 11	10	--	--	ns
t17	SYNC Delay After DATACLK High	9, 10, 11	15	--	35	ns
t18	Data Valid Delay	9, 10, 11	25	--	55	ns
t19	$\overline{CS}$ to Rising Edge Delay	9, 10, 11	25	--	--	ns
t20	Data Available after $\overline{CS}$ LOW	9, 10, 11	6	--	--	µs

Table 15. 7809LP Conversion Data Timing

Description	Analog Input						Digital Output			
							Binary Two's Complement (SB/$\overline{BTC}$ LOW)		Straight Binary (SB/$\overline{BTC}$ High)	
							Binary Code	Hex Code	Binary Code	Hex Code
Full Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305 µV	153 µV	102 µV	153 µV	76 µV	61 µV				
+ Full Scale (FS - 1 LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999938V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Mid-scale	-305 µV	-153 µV	-102 µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
-Full Scale	-10V	-5V	3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE 16. LPT™ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNIT
Supply Threshold	ITHR	75	ma
Protection Time	TPT	10	us
Supply Recovery Time	TSR	50	us
Functional Recoverty Time	TFR	75	us
8-Bit Accuracy Recovery Time	T8R	80	us
Full Scale Recovery Time	TFAR	5	ms

FIGURE 1. CONVERSION TIMING

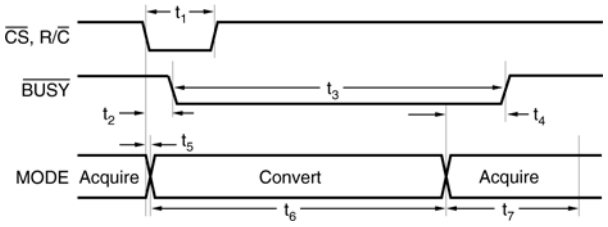


FIGURE 2. SERIAL DATA TIMING USING INTERNAL CLOCK ($\overline{CS}$, EXT/$\overline{INT}$ AND TAG TIED LOW)

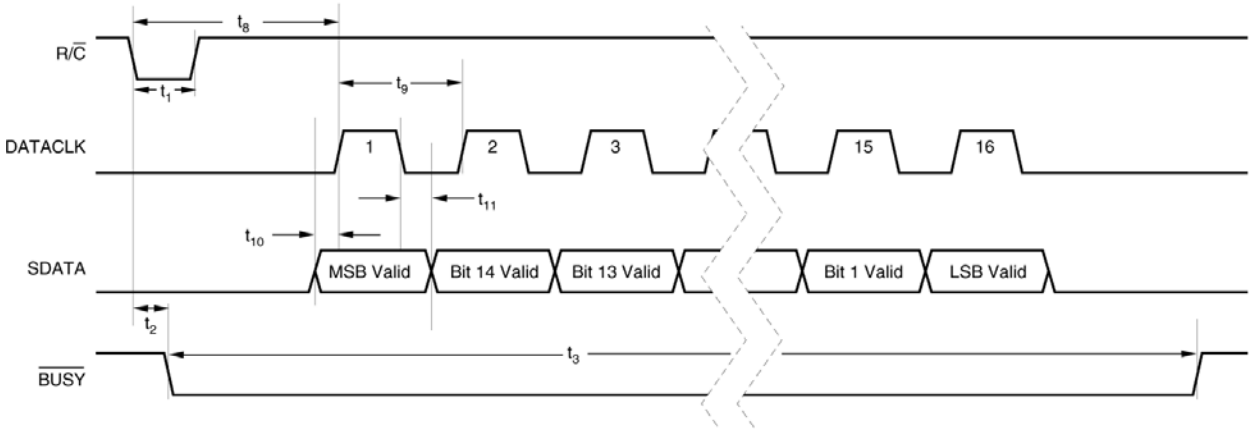


FIGURE 3. CONVERSION AND READ TIMING WITH EXTERNAL CLOCK (EXT/INT TIED HIGH). READ AFTER CONVERSION

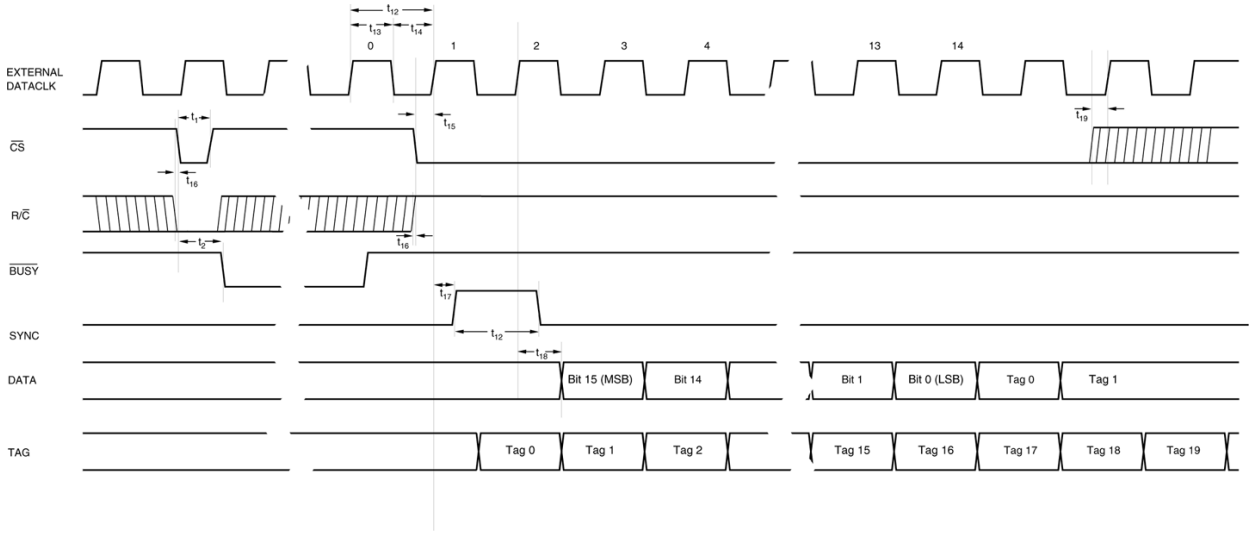


FIGURE 4. CONVERSION AND READ TIMING WITH EXTERNAL CLOCK (EXT/INT TIED HIGH). READ DURING CONVERSION

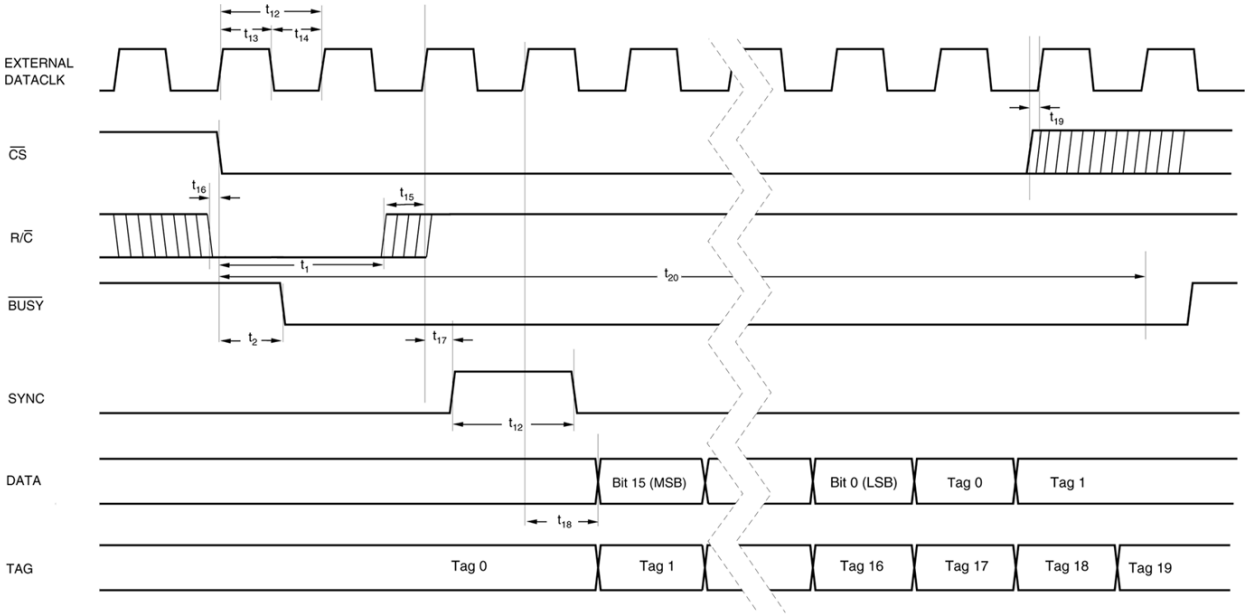


FIGURE 5. OFFSET/GAIN CIRCUITS FOR UNIPOLAR INPUT RANGES

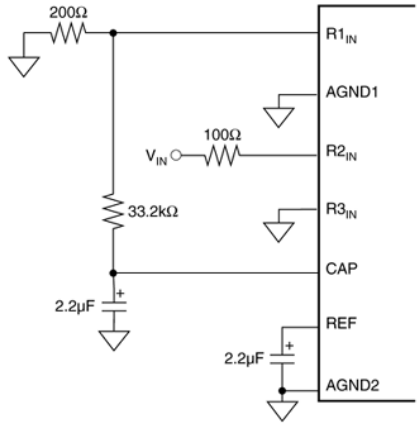
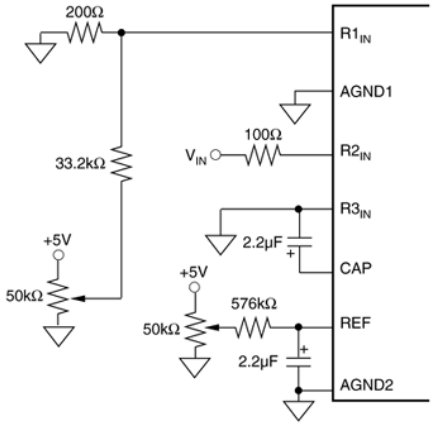
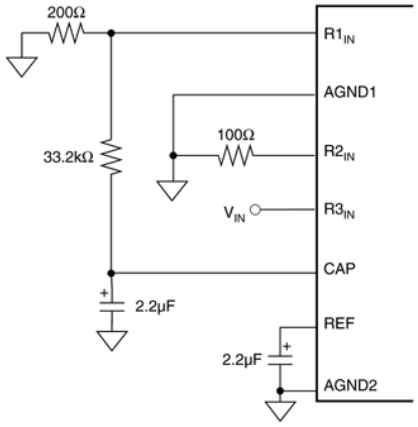
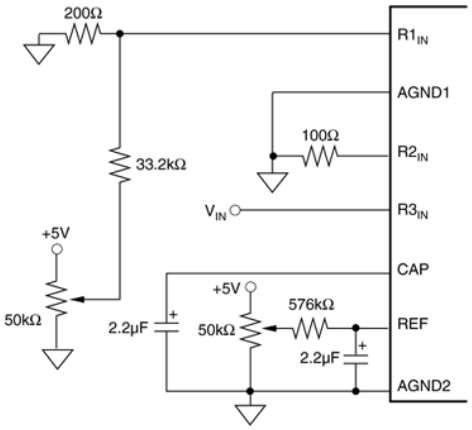
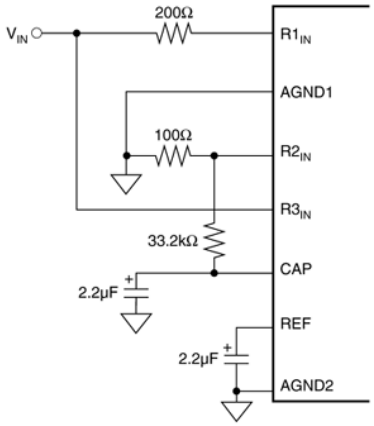
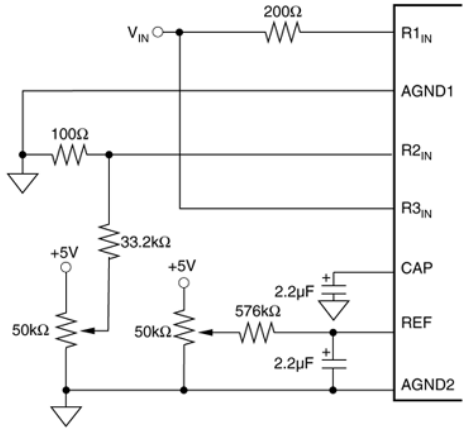
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

FIGURE 6. OFFSET/GAIN CIRCUITS FOR BIPOLAR INPUT RANGES

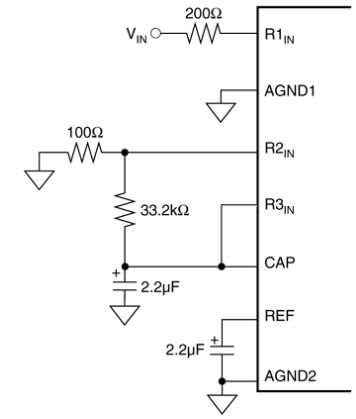
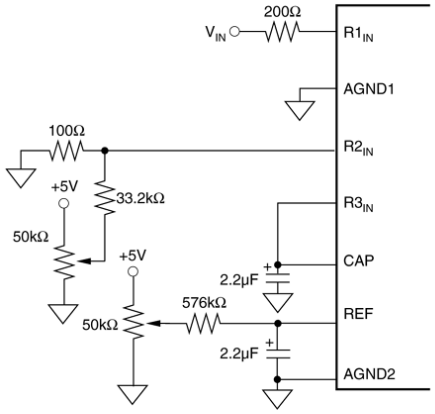
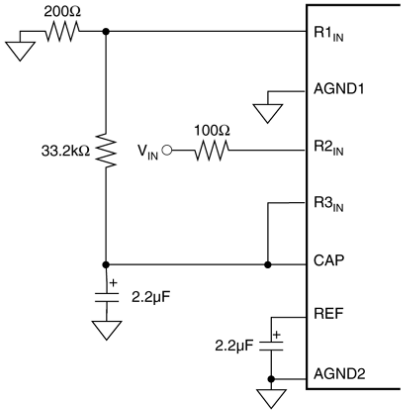
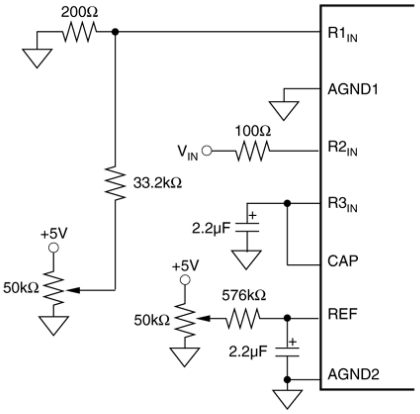
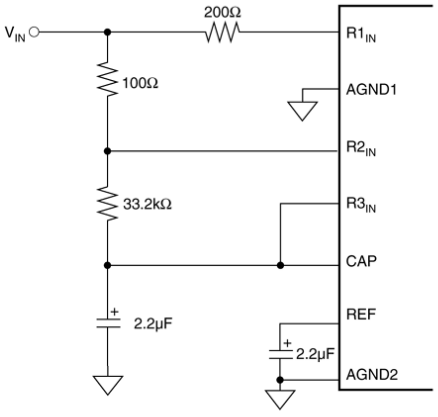
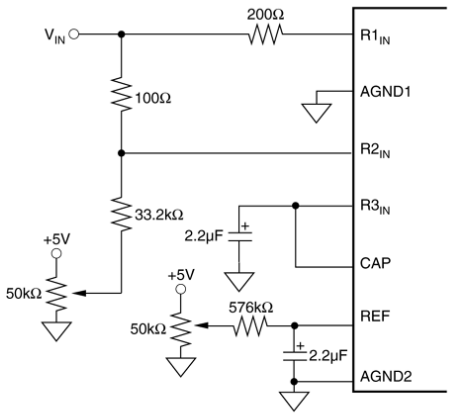
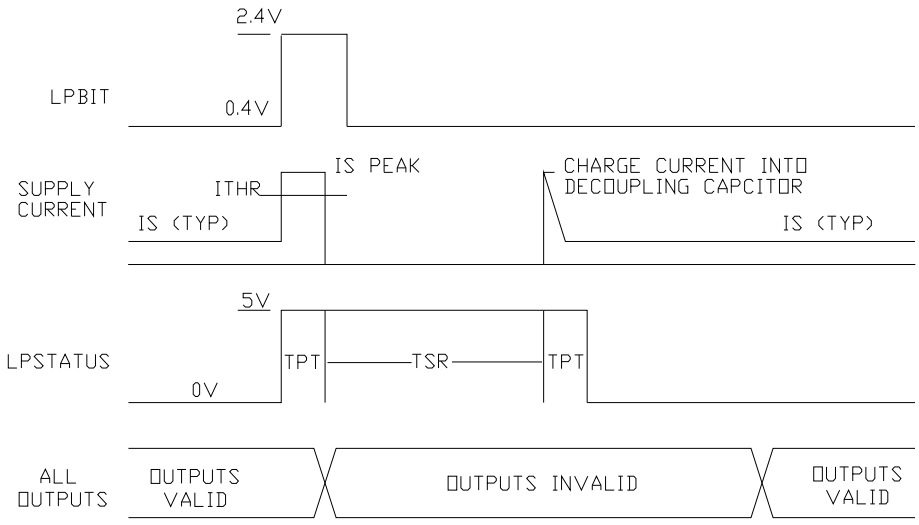
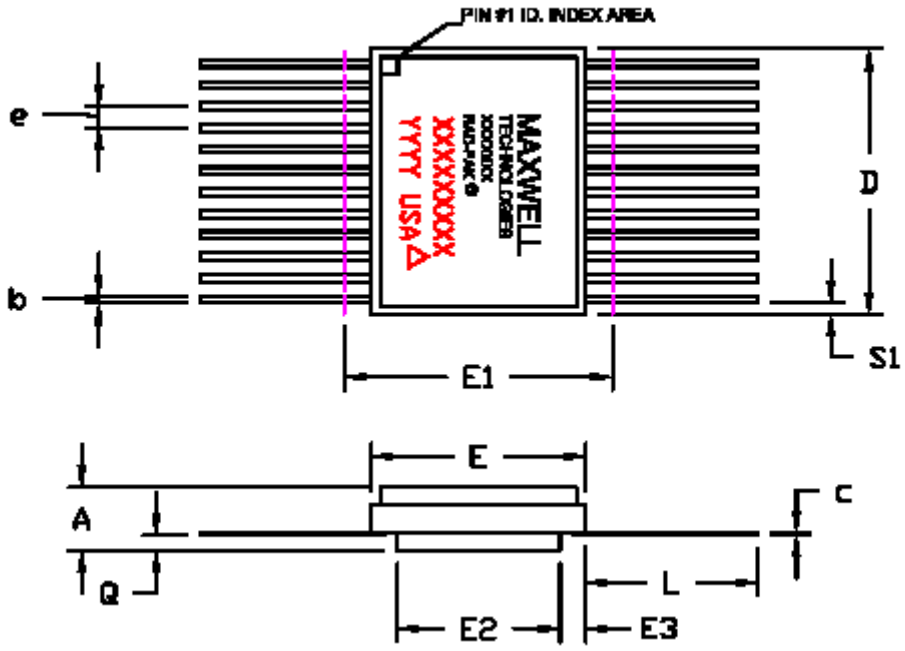
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

Figure 7. LPT™ Timing Diagram





24-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.255	0.278	0.302
b	0.015	0.017	0.022
c	0.006	0.008	0.010
D	--	0.596	0.640
E	0.390	0.400	0.410
E1	--	--	0.440
E2	0.268	0.270	0.272
E3	0.055	0.065	--
e		0.050 BSC	
L	0.420	0.430	0.450
Q	0.040	0.045	0.050
S1	0.006	0.014	--
N		24	

Note: All dimensions in inches
Top and Bottom of package internally connected to ground.

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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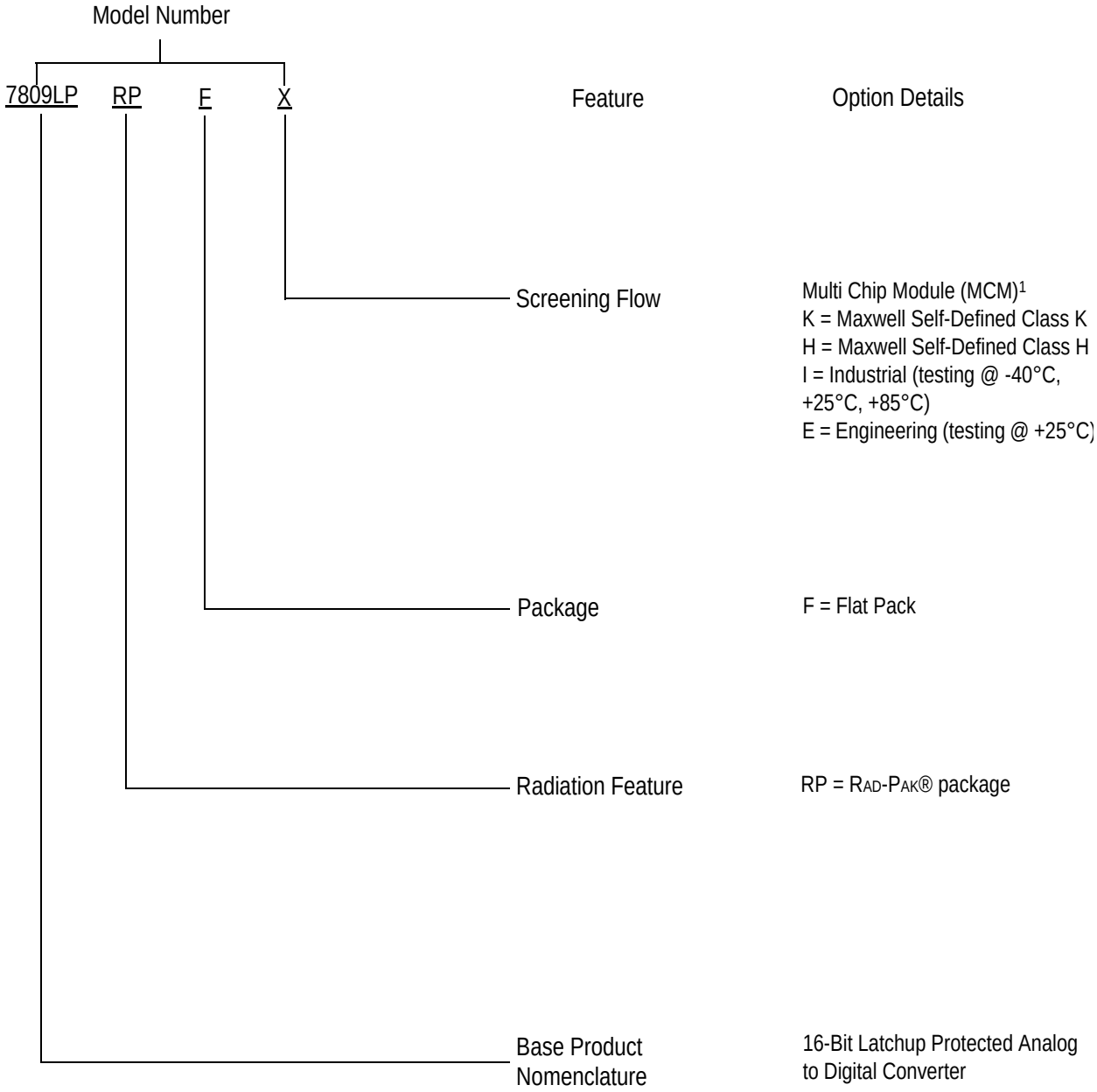
Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

Product Ordering Options



1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.