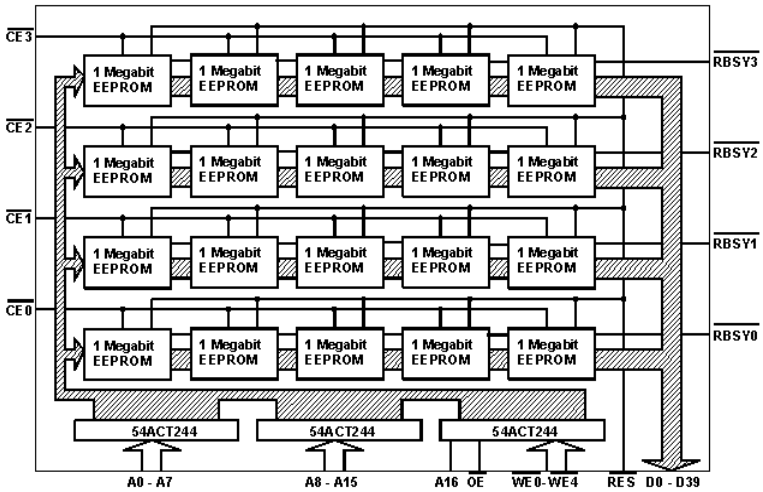
79LV2040B
20 Megabit (512K x 40-Bit) Low Low Voltage EEPROM MCM



Logic Diagram

FEATURES:

- 512k x 40-bit EEPROM MCM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - >100 krad (Si)
  - Dependent upon orbit
- Excellent Single event effects @ 25°C
  - SEL > 120 MeV cm²/mg (Device)
  - SEU > 85 MeV cm²/mg(Memory Cells)
  - SEU > 18 MeV cm²/mg (Write Mode)
  - SET > 40 MeV cm²/mg (Read Mode)
- High endurance
  - 10,000 cycles (Page Programming Mode)
  - 10 year data retention
- Page Write Mode: 128 Dword Page
- High Speed:
  - 200 and 250 ns maximum access times
- Automatic programming
  - 15 ms automatic Page/Dword write
- Low power dissipation
  - 100 mW/MHz active current
  - 1.5 mW standby current

DESCRIPTION:

Maxwell Technologies' 79LV2040B multi-chip module (MCM) memory features a greater than 100 krad (Si) total dose tolerance, dependent upon orbit. Using Maxwell Technologies' patented radiation-hardened RAD-PAK® MCM packaging technology, the 79LV2040B is the first radiation-hardened 20 megabit MCM EEPROM for space applications. The 79LV2040B uses twenty 1 Megabit high speed CMOS EEPROM die to yield a 20 megabit product. The 79LV2040B is capable of in-system electrical byte and page programmability. It has a 128 x 40 page programming function to make the erase and write operations faster. It also features Data Polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 79LV2040B, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC optional standard algorithm.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies' self-defined Class K

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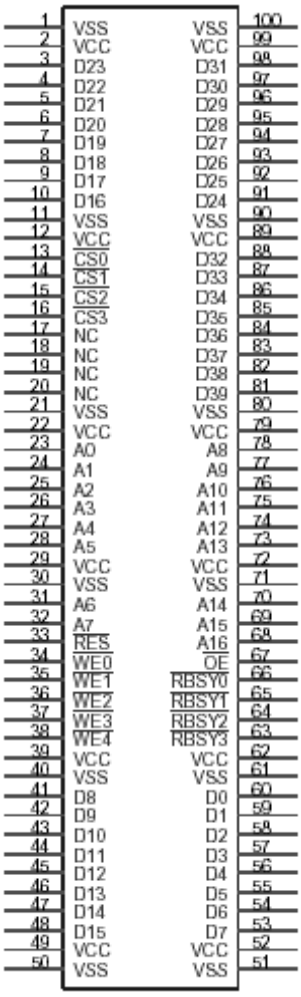

PINOUT DESCRIPTION

1, 11, 21, 30, 40, 50, 51, 61, 71, 80, 90, 100	**VSS - Ground**
2, 12, 22, 29, 39, 49, 52, 62, 72, 79, 89, 99	**VCC - Positive Supply**
60 - 53, 41 - 48, 10 - 3, 91 - 98, 88 - 81	**D0 to D39 Data I/O**
13, 14, 15, 16	**CS0\ - CS3\ Chip Enable**
23 - 28, 31, 32, 78 -73, 70 - 68	**A0 to A16 Address Inputs**
33	**RES\ - Reset**
34 - 38	**WE\0 - WE\4 Write Enables**
66 - 63	**RBSY\0 - RBSY\3 Ready/Busy**
67	**OE\ - Output Enable**

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TABLE 1. 79LV2040B ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	-0.6		7.0	V
Input Voltage	V_{IN}	-0.5[1]		7.0	V
Package Weight	RP		--		Grams
Operating Temperature Range	T_{OPR}	-55		125	˚C
Storage Temperature Range	T_{STG}	-65		150	˚C

1. V_{IN} min = -3.0V for pulse width ≤50ns.

TABLE 2. 79LV2040B RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	3.0	3.6	V
Input Voltage	V_{IL}	-0.3[1]	0.8	V
	V_{IH}	2.2	V_{CC} +0.3	V
$\overline{RES}$_PIN	V_H	V_{CC}-0.5	V_{CC} +1	V
Operating Temperature Range	T_{OPR}	-55	125	˚C

1. V_{IL} min = -1.0V for pulse width ≤ 50 ns

TABLE 3. 79LV2040B DELTA LIMITS[1]

PARAMETER	VARIATION
I_{CC1A}	+/- 10 % Specified in Table 5
I_{CC1B}	+/- 10 % Specified in Table 5
I_{CC2A}	+/- 10 % Specified in Table 5
I_{LI} - ADDR, CE, OE, WE	+/- 10 % Specified in Table 5
I_{LI} - D0-D39	+/- 10 % Specified in Table 5

1. Parameters are measured and recorded as Deltas per MIL-STD-883 for Class K Devices.

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TABLE 4. 79LV2040B CAPACITANCE

(T_A = 25 ˚C, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance : V_{IN} = 0V[1]	C_{IN} $\overline{OE}$		6	pF
	C_{IN} WE		6	
	C_{IN} $\overline{CE}_{0-30}$		30	
	C_{IN} A0-A16		6	
	C_{IN} RES		120	
Output Capacitance: V_{OUT} = 0V[1]	C_{Out} RDY/$\overline{BSY}$		60	pF
	$C_{O\,ut}$ D0-D39	--	48	

1. Guaranteed by design.

TABLE 5. 79LV2040B DC ELECTRICAL CHARACTERISTICS

(V_{cc} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Input Leakage Current A0-A16,$\overline{WE}$, $\overline{OE}$	V_{IN} = V_{CC} & 0V	I_{LI}	1, 2, 3	--	2	µA
Input Leakage Current $\overline{CE}$	V_{IN} = V_{CC} & 0V				10	uA
Input Leakage Current D0-D39	V_{IN} = V_{CC} & 0V	I_{LI}	1, 2, 3		10	µA
Output Leakage Current	(V_{CC} = 3.6V, V_{OUT} = 3.6V/0.4V)	I_{LO}	1, 2, 3	--	8	µA
Standby V_{CC} Current	$\overline{CE}$ = ADDR=$\overline{WE}$=$\overline{OE}$ =V_{CC}	I_{CC1A}	1, 2, 3	--	640	µA
	$\overline{CE}$ = $V_{IH;}$ ADDR=WE=OE =V_{CC}	I_{CC1B}			21	mA
Operating V_{CC} Current,	$\overline{OE}$ = 0V ADDR=$\overline{WE}$=V_{CC} I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 1 us at V_{CC} = 3.6V	I_{CC2A}	1, 2, 3		30	mA
	$\overline{OE}$ =ADDR=$\overline{WE}$=0V I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 150 ns at V_{CC} =3.6V	I_{CC2D}	1, 2, 3		75	mA
Input Voltage $\overline{RES}$_PIN		V_{IL} V_{IH} V_H	1, 2, 3	 2.2 V_{CC} -0.5	0.8	V
Output Voltage	Data Lines: V_{CC}Min, I_{OL}= 2.1mA Data Lines: V_{CC} Min, I_{OH} = -400µA All Outputs: V_{CC}Min , I_{OH} = -100uA	V_{OL} V_{OH} V_{OH}	1, 2, 3	-- 2.4 V_{CC} - 0.3V	0.4 -- --	V V V

1) For RES IIL=2000uA max.

2) Only one $\overline{\text{Chip Enable}}$ Active (Logic Low) at a time.

3) $\overline{RDY/BSY}$ is an open drain output. Only V_{OL} applies to this pin.

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TABLE 6. 79LV2040B AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION [1]

(V_{CC} =3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Address Access Time $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	t_{ACC}	9, 10, 11			ns
-200			--	200	
-250			--	250	
Chip Enable Access Time $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	t_{CE}	9, 10, 11			ns
-200			--	200	
-250			--	250	
Output Enable Access TIme $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	t_{OE}	9, 10, 11			ns
-200			0	110	
-250			0	120	
Output Hold to Address Change $\overline{CE}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ = V_{IH}	t_{OH}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Output Disable to High-Z [2]		9, 10, 11			
$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	t_{DF}				ns
-200			0	50	
-250			0	50	
$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	t_{DFR}				ns
-200			0	300	
-250			0	350	
$\overline{RES}$ to Output Delay $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} [3]	t_{RR}	9, 10, 11			ns
-200			0	525	
-250			0	600	

1. Test conditions: input pulse levels = 0.4V to 2.4V; input rise and fall times ≤ 20 ns; output load = 1 TTL gate + 100 pF (including scope and jig); reference levels for measuring timing = 0.8 V/1.8 V.
2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

TABLE 7. 79LV2040B AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATION

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN [1]	MAX	UNITS
Address Setup Time	t_{AS}	9, 10, 11			ns
-150			0	--	
-200			0	--	
Chip Enable to Write Setup Time ($\overline{WE}$ controlled)	t_{CS}	9, 10, 11			ns
-150			0	--	
-200			0	--	

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TABLE 7. 79LV2040B AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATION

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN [1]	MAX	UNITS
Write Pulse Width		9, 10, 11			
$\overline{CE}$ controlled	t_{CW}				ns
-200			200	--	
-250			250	--	
$\overline{WE}$ controlled	t_{WP}				ns
-200			200	--	
-250			250	--	
Address Hold Time	t_{AH}	9, 10, 11			ns
-200			125	--	
-250			125	--	
Data Setup Time	t_{DS}	9, 10, 11			ns
-200			100	--	
-250			150	--	
Data Hold Time	t_{DH}	9, 10, 11			ns
-200			10	--	
-250			10	--	
Chip Enable Hold Time ($\overline{WE}$ controlled)	t_{CH}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Write Enable to Write Setup Time ($\overline{CE}$ controlled)	t_{WS}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Write Enable Hold Time ($\overline{CE}$ controlled)	t_{WH}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Output Enable to Write Setup Time	t_{OES}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Output Enable Hold Time	t_{OEH}	9, 10, 11			ns
-200			0	--	
-250			0	--	
Write Cycle Time [2]	t_{WC}	9, 10, 11			ms
-200			--	15	
-250			--	15	
Data Latch Time	t_{DL}	9, 10, 11			ns
-200			700	--	
-250			750	--	
Byte Load Window	t_{BL}	9, 10, 11			µs
-200			100	--	
-250			100	--	
Byte Load Cycle	t_{BLC}	9, 10, 11			µs
-200			1	30	
-250			1	30	

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TABLE 7. 79LV2040B AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATION

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN [1]	MAX	UNITS
Time to Device Busy	t_{DB}	9, 10, 11			ns
-200			100	--	
-250			120	--	
Write Start Time [3]	t_{DW}	9, 10, 11			ns
-200			150	--	
-250			250	--	
$\overline{RES}$ to Write Setup Time	t_{RP}	9, 10, 11			µs
-200			100	--	
-250			100	--	
V_{CC} to $\overline{RES}$ Setup Time[4]	t_{RES}	9, 10, 11			µs
-200			1	--	
-250			1	--	

1. Use this device in a longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{BUSY}$ are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{BUSY}$ are used.
4. Guaranteed by design.

TABLE 8. 79LV2040B MODE SELECTION [1]

PARAMETER	$\overline{CE}$ [2]	$\overline{OE}$	$\overline{WE}$	I/O	$\overline{RES}$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	High-Z
Standby	V_{IH}	X	X	High-Z	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	High-Z --> V_{OL}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out[3]	V_H	V_{OL}
Program Reset	X	X	X	High-Z	V_L	High-Z

1. Refer to the recommended DC operating conditions.
2. For $\overline{CE}_{0-3}$ only one $\overline{CE}$ can be used ("on") at a time.
3. Bits 7, 15, 23, 31 and 39

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FIGURE 1. READ TIMING WAVEFORM

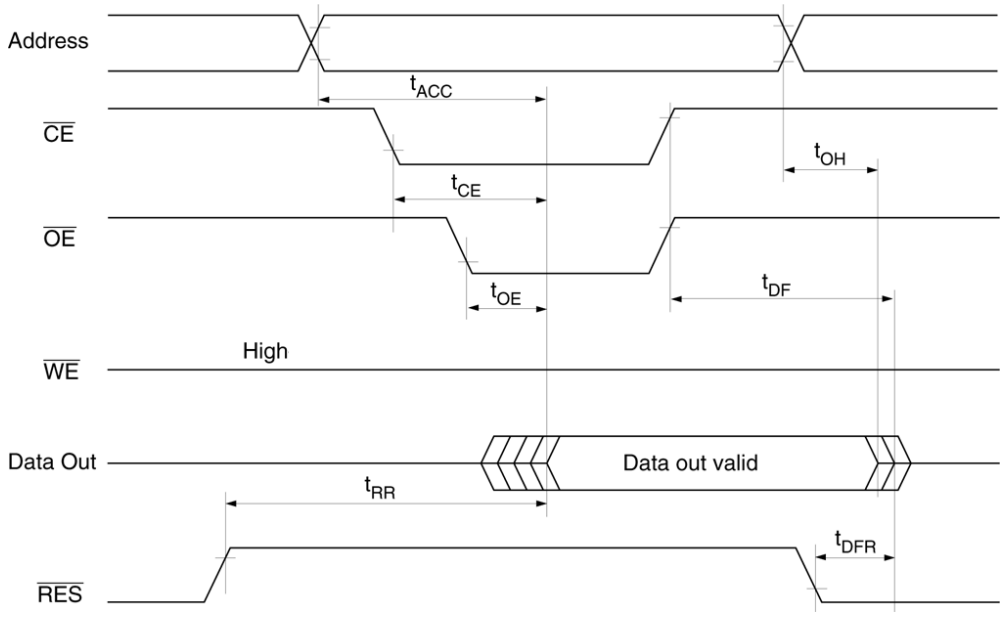

FIGURE 2. BYTE WRITE TIMING WAVEFORM (1) ($\overline{WE}$ CONTROLLED)

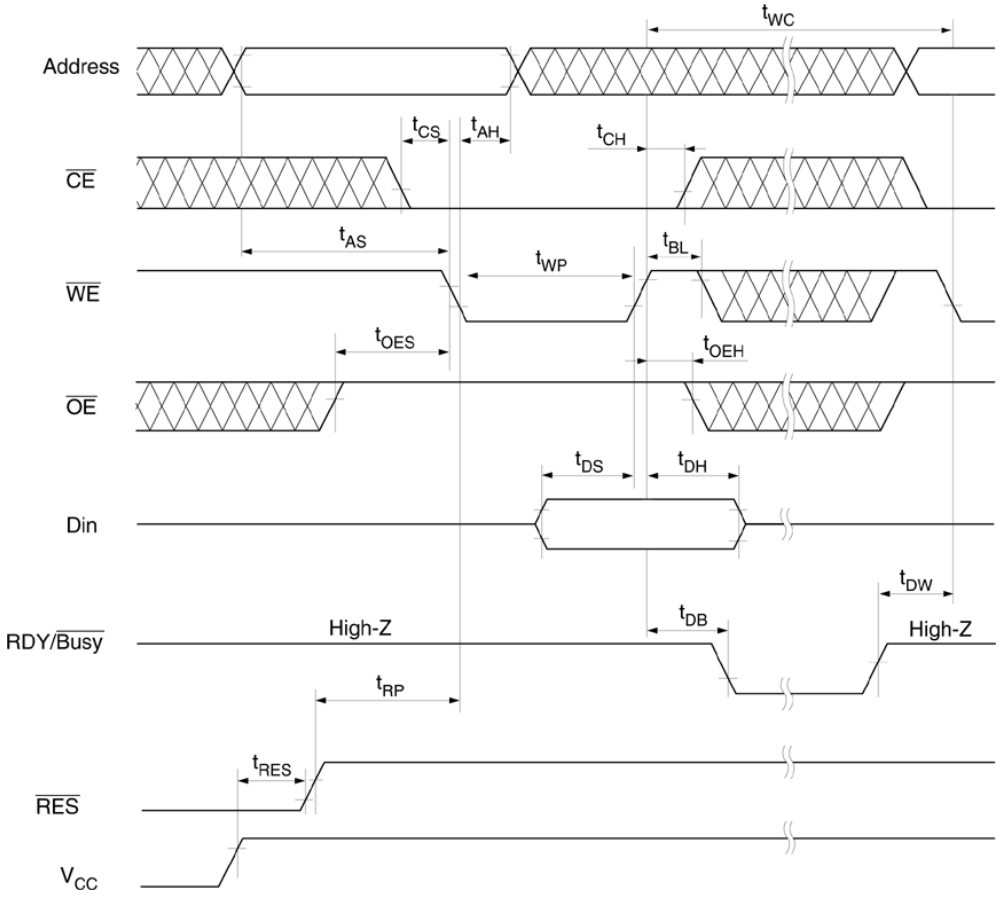

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FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

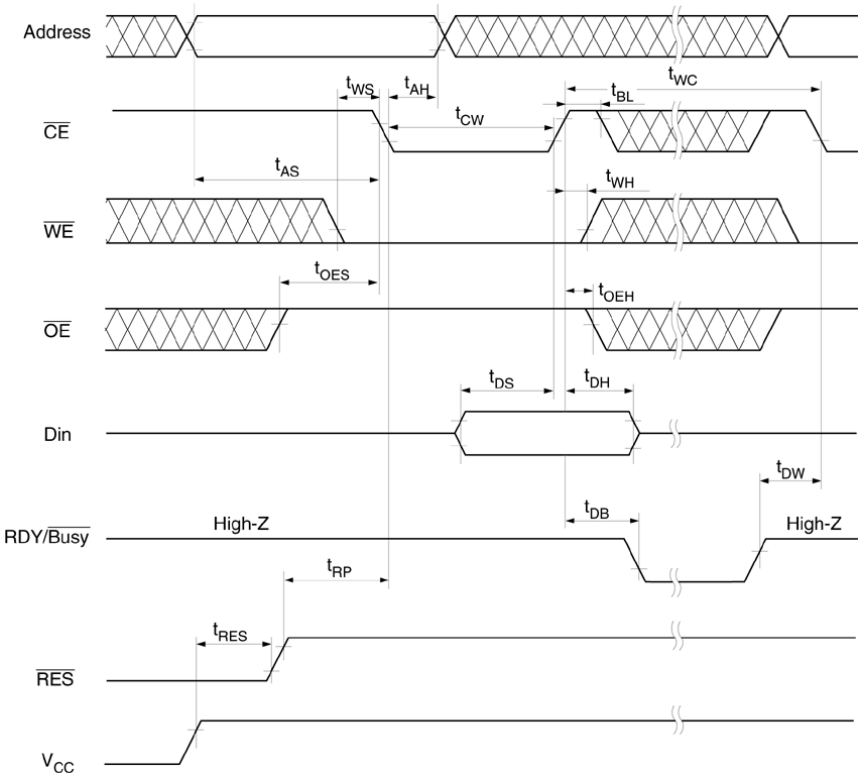
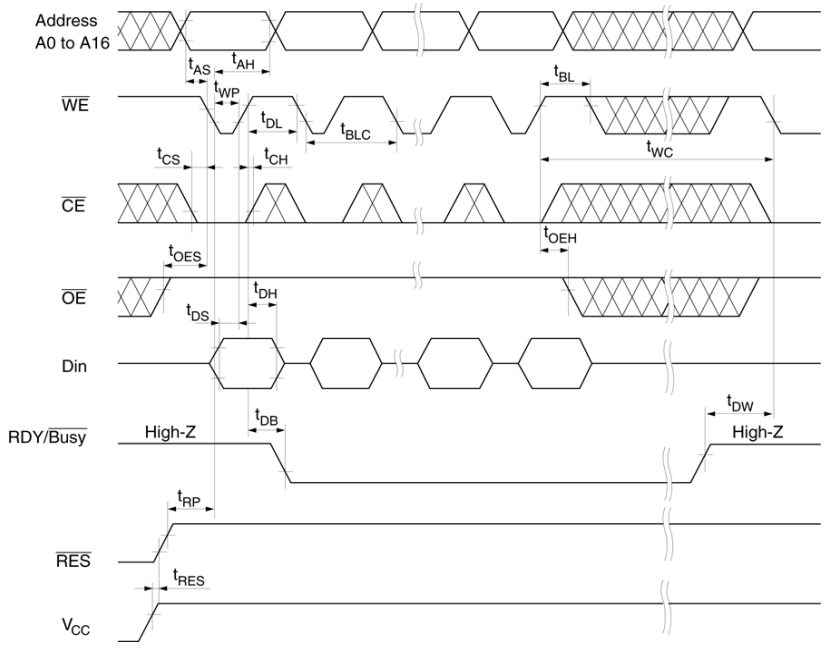


FIGURE 4. PAGE WRITE TIMING WAVEFORM (1) ($\overline{WE}$ CONTROLLED)



1) A7-A16 are Page Addresses and must be the same within a Page Write Operation.

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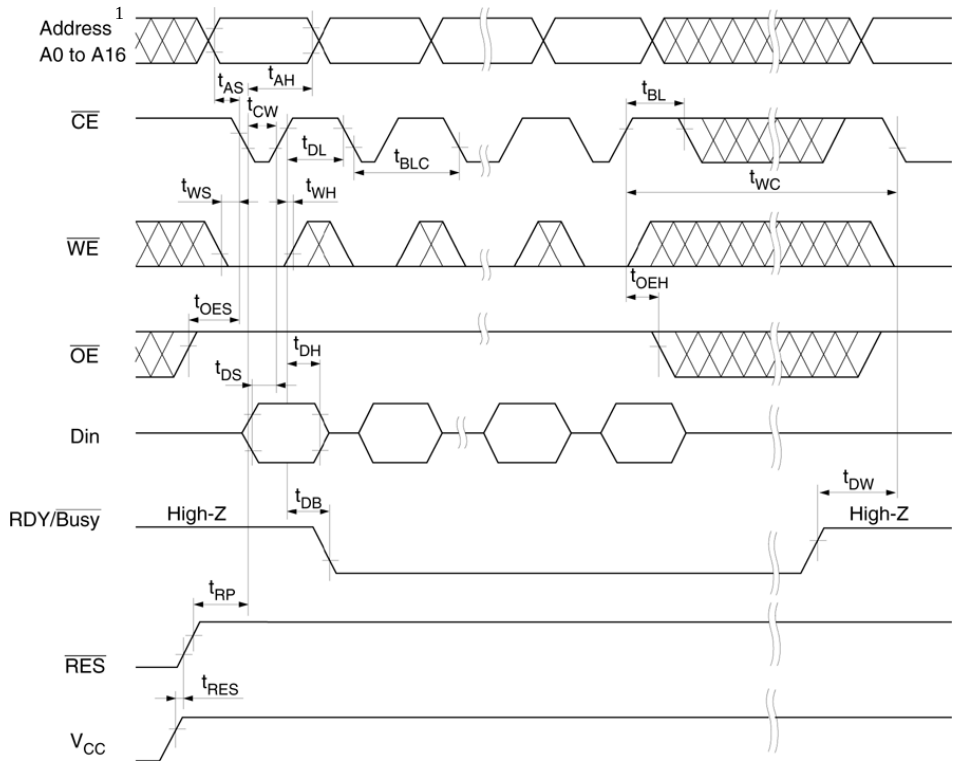
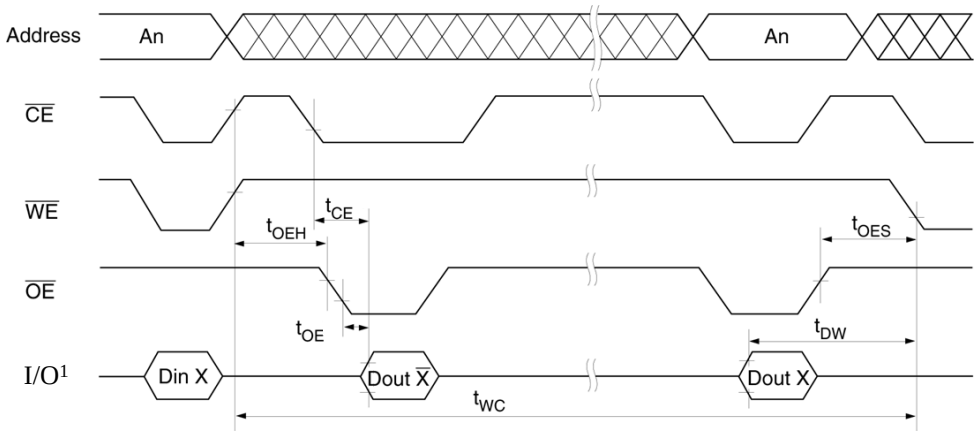
FIGURE 5. PAGE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)



1) A7-A16 are Page Addresses and must be the same within a Page Write Operation.

FIGURE 6. $\overline{DATA}$ POLLING TIMING WAVEFORM



1) BITS 7, 15, 23, 31 AND 39

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FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM (1) (IN PROTECTION MODE)

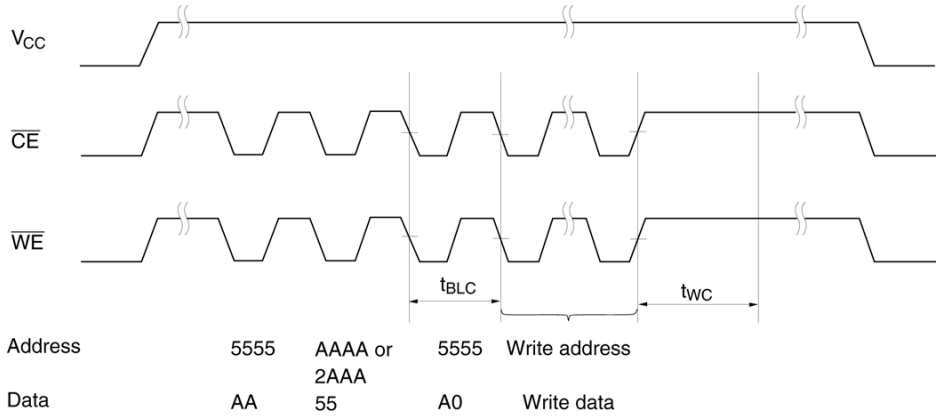
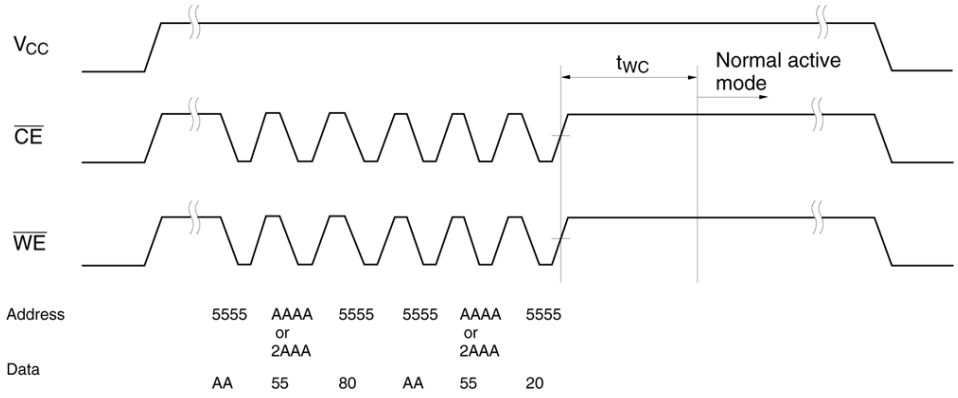


FIGURE 8. SOFTWARE DATA PROTECTION WAVEFORM (2) (IN NON-PROTECTION MODE)



EEPROM APPLICATION NOTES

This application note describes the programming procedures for the EEPROM modules and with details of various techniques to preserve data integrity.

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Loading the first byte of data, the data load window opens 30µs for the second byte. In the same manner each additional byte of data can be loaded within 30µs of the preceding falling edge of either $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ and $\overline{WE}$ are kept high for 100µs after data input, the EEPROM enters the write mode automatically and the data input is written into the EEPROM.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

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Data Polling

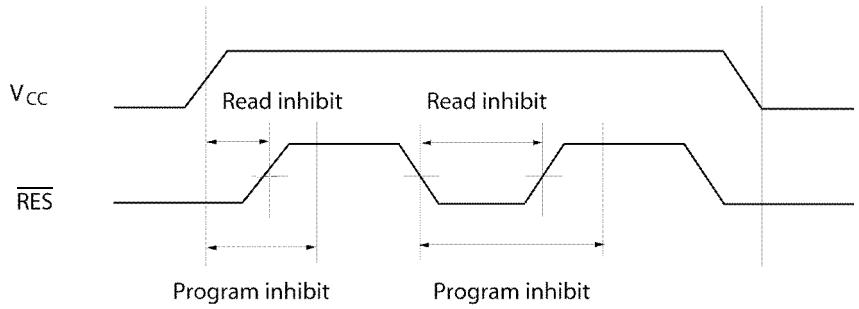
Data Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O 7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows a comparison operation to determine the status of the EEPROM. The RDY/$\overline{\text{Busy}}$ signal goes low ($V_{OL)}$ after the first write signal. At the end of the write cycle, the RDY/Busy returns to a high state (V_{OH}).

$\overline{\text{RES}}$ Signal

When $\overline{\text{RES}}$ is LOW (V_L), the EEPROM cannot be read or programmed. The EEPROM data must be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is power on and off. $\overline{\text{RES}}$ should be high (V_H) during read and programming operations.

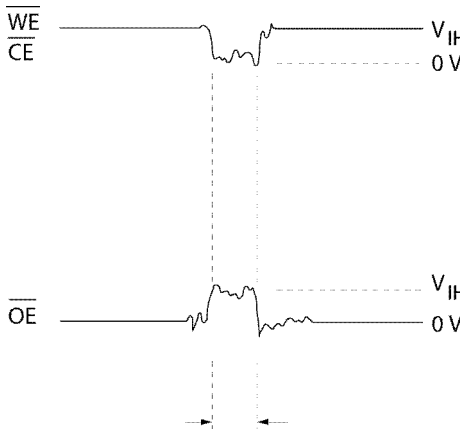


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

1. Data Protection against Noise of Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation.

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width more than 20ns on the control pins.



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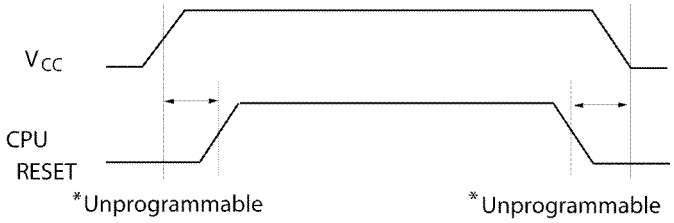
2. Data Protection at V_{CC} on/off

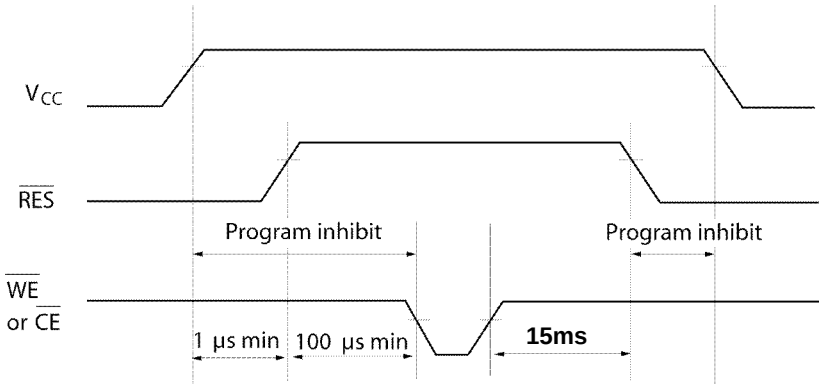
When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to $\overline{RES}$ pin.



3. $\overline{RES}$ Signal

$\overline{RES}$ should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when $\overline{RES}$ become low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data is input

.



4. Software Data Protection Enable

The 79LV2040A contains a software controlled write protection feature that allows the user to inhibit all write operations to the device. This is useful in protecting the device from unwanted write cycles due to uncontrollable circuit noise or inadvertent writes caused by minor bus contentions. Software data protection is enabled by writing the following data sequence to the EEPROM and allowing the write cycle period (t_{WC}) of 15ms to elapse:

.

Software Data Protection Enable Sequence

Address	Data
5555	AA AA AA AA AA
AAAA or 2AAA	55 55 55 55 55
5555	A0 A0 A0 A0 A0

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5. Writing to the Memory with Software Data Protection Enabled

To write to the device once Software protection is enabled, the enable sequence must precede the data to be written. This sequence allows the write to occur while at the same time keeping the software protection enabled

Sequence for Writing Data with Software Protection Enabled.

Address	Data
5555	AA AA AA AA AA
AAAA or 2AAA	55 55 55 55 55
5555	A0 A0 A0 A0 A0
Write Address(s)	Normal Data Input

6. Disabling Software Protection

Software data protection mode can be disabled by inputting the following 6 bytes sequence. Once the software protection sequence has been written, no data can be written to the memory until the write cycle (T_{WC}) has elapsed.

Software Protection Disable Sequence

Address	Data
5555	AA AA AA AA AA
AAAA or 2AAA	55 55 55 55 55
5555	80 80 80 80 80
5555	AA AA AA AA AA
AAAA or 2AAA	55 55 55 55 55
5555	20 20 20 20 20

Devices are shipped in the “unprotected” state, meaning that the contents of the memory can be changed as required by the user. After the software data protection is enabled, the device enters the Protect Mode where no further write commands have any effect on the memory contents.

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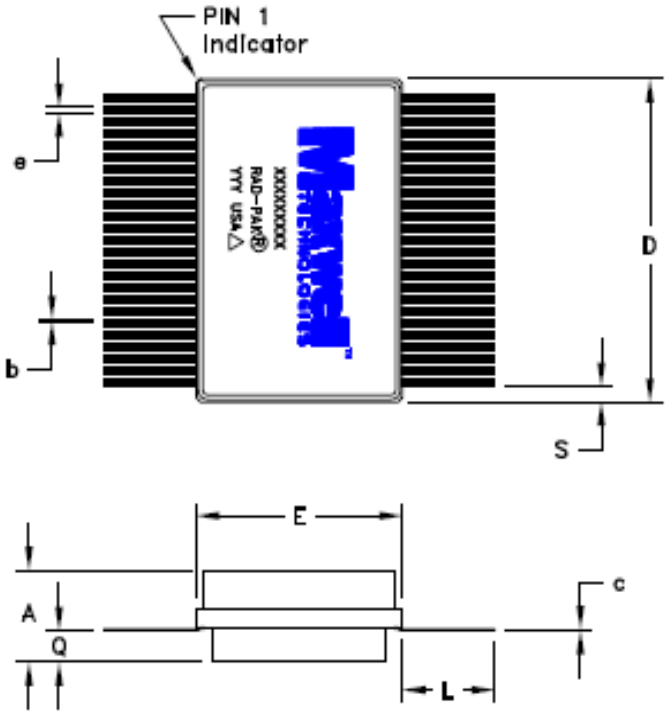

100 Pin Rad-Tolerant Flat Pack

Symblol	Dimensions		
	Min	Nom	Max
A	0.381	0.400	0.419
b	0.006	0.008	0.010
c	0.005	0.006	0.007
D	1.351	1.366	1.381
e		0.025 BSC	
E	0.887	0.897	0.907
L	0.390	0.400	0.410
Q	0.132	0.139	0.147
S	0.055	0.075	0.095
A	0.381	0.400	0.419
b	0.006	0.008	0.010

Note: All dimensions in inches.
Top and Bottom of the package is internally connected to ground.

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Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

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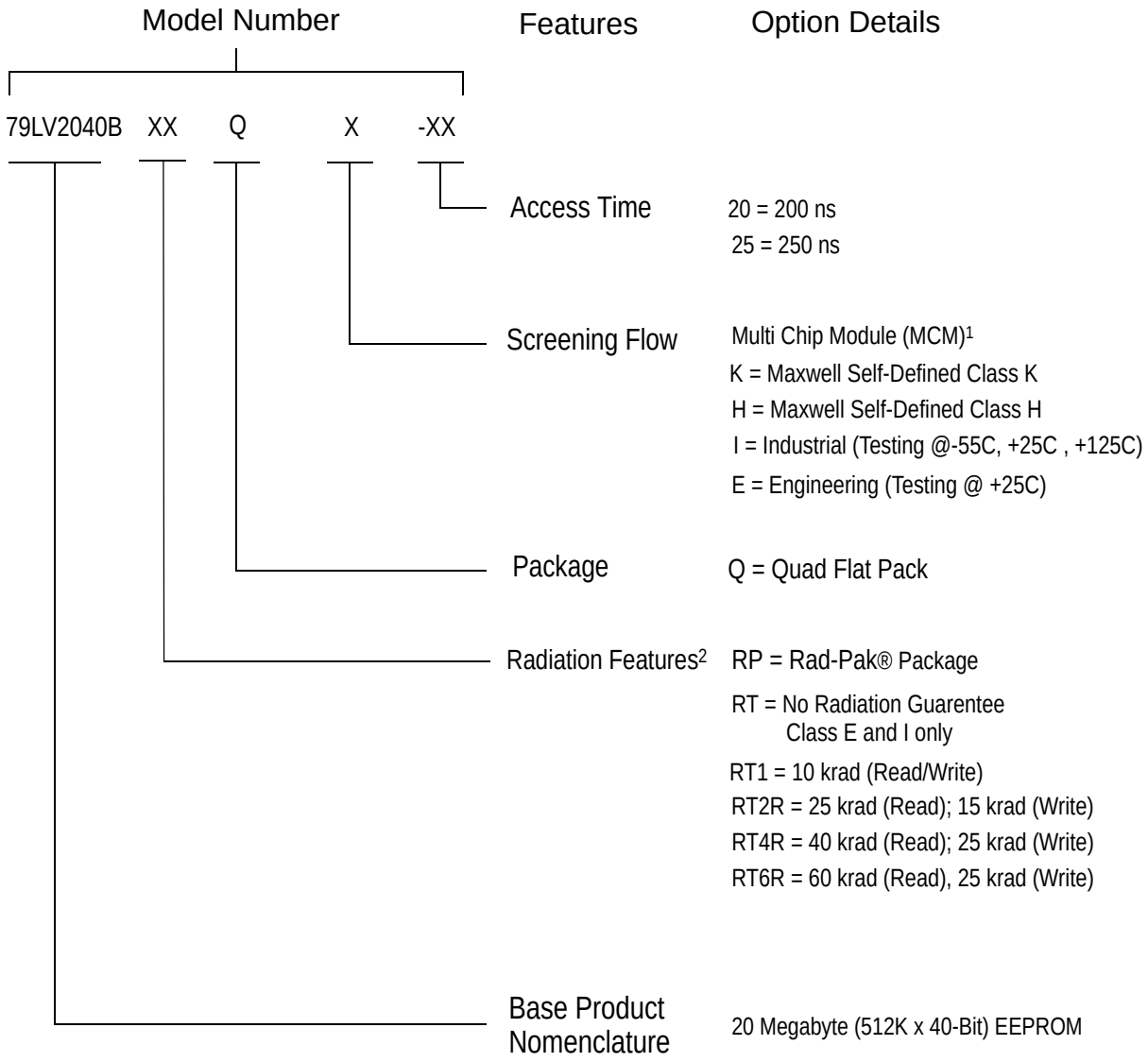
Product Ordering Options



1) Products are manufacturered and screened to Maxwell Technologies' self-defined Class H and Class K.

2) The device will meet the specified read mode TID level, at the die level, if it is not written to during irradiation. Writing to the device during irradiation will reduce the device's TID tolerance to the specified write mode TID level. Writing to the device before irradiation does not alter the device's read mode TID level.

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