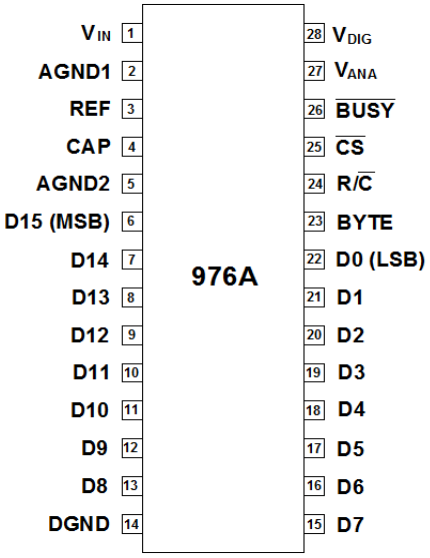
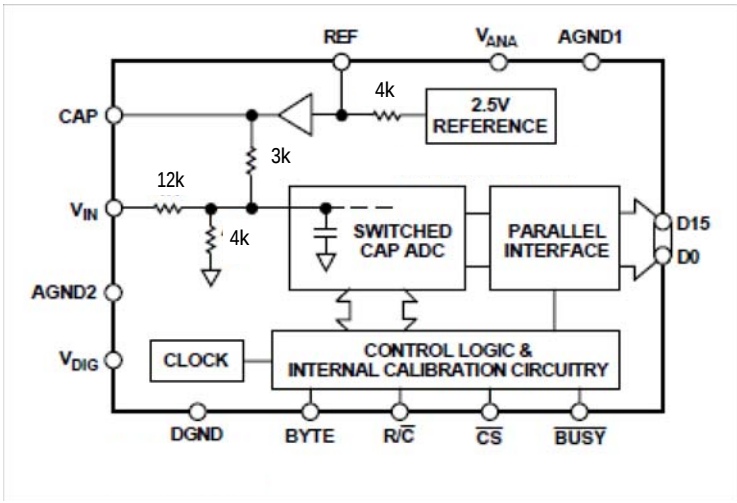
976A
16-Bit Analog to Digital Converter





Functional Block Diagram

FEATURES:

- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  > 100 krad (Si), depending upon space mission
- SEE Performance:
  SEL and SEFI immune at LET = 85MeV cm^2 and 125°C
- Package: 28 pin RAD-PAK® flat package
- 200 kHz max sampling rate
- Data Coding - Binary Twos Compliment
- ±10 V input range
- Single +5 V supply operation
- Utilizeses an internal or external reference
- Power dissipation: 100 mW max

DESCRIPTION:

Maxwell Technologies' 976A high-speed 16-bit analog to digital converter, features a greater than 100 krad (Si) total dose tolerance depending upon space mission, using Maxwell's radiation-hardened RAD-PAK® packaging technology. It is a 28 pin, 16-bit sampling analog to digital converter using state-of-the-art BiCMOS structures. The 976A contains a 16-bit capacitor based SAR A/D with S/H, reference, clock and interface for microprocessor use. The 976A is specified at a 200 kHz sampling rate, and guaranteed over the full temperature range.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies' self-defined Class S.

TABLE 1. 976A PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{IN}	Analog Input. Connect a 200 ohm resistor between V_{IN} and the analog signal source. Full scale input range is ±10V.
2	AGND1	Analog Ground. Used as ground reference point for REF pin..
3	REF	Reference Input/Output. The internal +2.5V reference is available at this pin. Alternatively, an external reference can be used to override the internal reference. In either case, connect a 2.2uF tantalum capacitor between REF and AGND1.
4	CAP	Referenced buffer Output. Connect a 2.2uF tantalum capacitor between CAP and AGND2.
5	AGND2	Analog Ground.
6	D15(MSB)	Data Bit 15. Most significant bit of conversion result. High impedence state when $\overline{CS}$ is high or when R/$\overline{C}$ is Low.
7-13	D14-D8	Data bits 14 -8.High impedence state when $\overline{CS}$ high or when R/$\overline{C}$ is Low.
14	DGND	Digital Ground.
15-21	D7-D1	Data Bits D7-D1. High impedence state when $\overline{CS}$ is high or when R/$\overline{C}$ is Low.
22	D0(LSB)	Data Bit 0. High impedence state when $\overline{CS}$ is high or when R/$\overline{C}$ is Low.
23	BYTE	Byte Select. With Byte LOW, data will be output as indicated above; Pin 6 (D15) is the MSB, Pin 22 (D0) is the LSB. Wtih BYTE HIGH, the top and bottom 8 bits of data will be switched; D15-D8 are output on Pins 15-22 and D7-D0 are output on Pins 6-13.
24	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion; a rising edge enables the output data bits.
25	$\overline{CS}$	Chip Selet Input. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits. When $\overline{CS}$ is HIGH, the output data bits will be in the Hi-impedence state.
26	$\overline{BUSY}$	$\overline{Busy}$ output. Goes LOW when a conversion is started and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ tied LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises. The rising edge of $\overline{BUSY}$ can be used to latch the output data.
27	V_{ANA}	Analog Power Supply. Nominally +5V.
28	V_{DIG}	Digital Power Supply. Nominally +5V.

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TABLE 2. 976A ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAX	UNIT
Analog Inputs - V_{IN} - CAP - REF	 ±25 +VANA + 0.3V TO AGND2 - 0.3V Indefinite Short to Ground	V

TABLE 2. 976A ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAX	UNIT
Ground Voltage Differences: - DGND - AGND1 - AGND2	 ±0.3 ±0.3 ± 0.3	V
V_{ANA}	7	V
V_{DIG}	7	V
V_{DIG} to V_{ANA}	± 7	V
Digital Inputs	-0.3V to V_{DIG} + 0.3V	V
Junction Temperature	+150	˚C
Operating Temperature	-55 to +125	˚C
Weight	5.5	Grams
Thermal Resistance (Tjc)	1.3	˚C/W
Storage Temperature	-65 to +150	˚C

TABLE 3. 976A DC ACCURACY SPECIFICATIONS[1]

(SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Integral Linearity Error	1,2, 3	-3	--	+3	LSB [2]
Differential Linearity Error	1,2, 3	-1	--	4	LSB
No Missing Codes [3]	1, 2, 3	15	--	--	Bits
Transition Noise [4]		--	1.0	--	LSB
Full Scale Error [5,6]	1, 2, 3	-0.5	--	+0.5	%
Full Scale Error [5,6] (using ext. 2.5000 V_{ref})	1, 2, 3	-0.6		+0.6	%
Full Scale Error Drift	--		±7	--	ppm/˚C
Full Scale Error Drift (using ext. 2.5000 V_{ref})	--	--	±7	--	ppm/˚C
Bipolar Zero Error [5]	1, 2, 3	-10	--	+10	mV
Bipolar Zero Error Drift		--	±2	--	ppm/˚C
Power Supply Sensitivity	1,2, 3	-12	--	+8	LSB

1. Unless otherwise specified, V_{REF} = 2.5V, V_{IH} = 2.0V, V_{IL} = 0.8 V
2. LSB stands for Least Significant Bit. One LSB is equal to 305 µV.
3. Not tested.
4. Typical rms noise at worst case transitions and temperatures.
5. Measured with various fixed resistors.
6. For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last scale code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

Table 4. Delta Limits[1]

Parameter	Variation
I_{CC}	±10% per Table 10

1) Parameters are measured and recorded as Delts per MIL-STD-883 for Class S devices.

Table 5. Digital Inputs

Parameter	Sub-Groups	Min	Max	Units
Input Voltage V_{IL}[1]	1, 2, 3	-0.3	+0.8	V
Input Voltage V_{IH}[1]	1, 2, 3	+2.0	V_{DIG} +0.3	V
Input Current I_{IL}	1, 2, 3	-10	10	uA
Input Current I_{IH}	1, 2, 3	-10	10	uA

1. Tested by application of signal, V_{IL} at 0.8V, V_{IH} at 2.0V.

Digital Outputs

Specified Performance -55to +125°C, VDIG=VANA = 5V +/- 5%)

Parameter	Sub-Groups	Min	Max	Units
Data Formatting - 16 Bits				
Data Coding - Binay Twos Compliment				
V_{OL} @ 1.6mA	1, 2, 3		0.4	V
I_{OL}	1, 2, 3	-5	5	uA
V_{OH} @ 500uA	1, 2, 3	4		V
I_{OH}	1, 2, 3	-5	5	uA

Table 6. 976A Analog Input and Throughput Speed

Specified Performance -55to +125°C, VDIG=VANA = 5V +/- 5%)

Parameter	Subgroups	Min	Typ	Max	Unit
Voltage Ranges	--	-10		10	V
Impedance[1]	1, 2, 3	--	13	--	kohms
Capacitance[1]		--	22	--	pF
Output Capcitance[1]	1, 2, 3	--	--	15	pF
Complete Cycle (Acquire and Convert)	9, 10, 11	--	--	5	µs
Throughput Rate [2]	9, 10, 11	200	--	--	kHz

1. Not Tested.

2. Tested by application of signal at limit.

TABLE 7. 976A AC ACCURACY SPECIFICATIONS

SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, f_{IN} = 20 kHz [1]	4, 5, 6	90	--	--	dB [2]
Total Harmonic Distortion, f_{IN} = 20 kHz [1]	4, 5, 6	--	--	-90	dB
Signal-to-Noise (Noise + Distortion) [1] f_{IN} = 20 kHz -60 dB Input	4, 5, 6	83 --	-- 27	-- --	dB
Signal-to-Noise [1], f_{IN} = 20 kHz	4, 5, 6	83	--	--	dB
Full-Power Bandwidth [1,3]		--	1	--	MHz

1. Not Tested
2. All specifications in dB are referred to a full-scale ±10 V input.
3. Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-Noise (Noise + Distortion) degrades to 60 dB.

TABLE 8. 976A SAMPLING DYNAMICS

SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Input Bandwidth			2.7		MHz
Aperture Delay		--	40	--	ns
Aperture Jitter	9, 10, 11	Sufficient to meet AC specification			
Transient Response FS Step[2]	9, 10, 11	--	--	1	us
Overvoltage Recovery [1]		--	150	--	ns

1. Recovers to specified performance after 2 X FS input overvoltage.

2. Not Tested

TABLE 9. 976A REFERENCE

SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must be ext. buffer)		--	1	--	µA
External Reference Voltage Range for Specified Linearity [1]		--	2.5	--	V
External Reference Current Drain	2.30V & 2.70V	--	--	100	µA

1. Tested by application of signal at 2.5V +/- 0.02V.

TABLE 10. 976A POWER SUPPLIES

SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG}	1, 2, 3	Must be ≤ V_{ANA}	4.75	5	5.25	V
V_{ANA}	1, 2, 3		4.75	5	5.25	V
I_{DIG}	--		--	--	5	mA
I_{ANA}	--		--	--	15	mA
Icc	1, 2, 3	I_{DIG} + I_{ANA} @ 200kHz			20	mA
Power Dissipation	1, 2, 3	V_{ANA} = V_{DIG} = 5V f_s = 200 kHz	--	--	100	mW

TABLE 11. 976A CONVERSION AND DATA TIMING

SPECIFIED PERFORMANCE -55TO +125°C, VDIG=VANA = 5V +/- 5%)

SYMBOL	DESCRIPTION	SUBGROUPS	MIN	TYP	MAX	UNIT
t1[1]	Convert Pulse Width	9, 10, 11	50	--	--	ns
t2	Data Valid Delay after R/$\overline{C}$ Low	9, 10, 11	--	--	4.0	µs
t3	$\overline{BUSY}$ Delay	9, 10, 11	--	--	100	ns
t4	$\overline{BUSY}$ LOW	9, 10, 11	--	--	4.0	us
t5	$\overline{BUSY}$ Delay after End of Conversion	--	--	180	--	ns
t6	Aperture Delay	--	--	40	--	ns
t7[2]	Conversion Time	9, 10, 11	--	3.8	4.0	µs
t8[2]	Acquisition Time	9, 10, 11	1.0	--	--	µs
t9	Bus Relinquish Time	9, 10, 11	10	35	83	ns
t10	$\overline{BUSY}$ Delay after Data Valid	9, 10, 11	50	180	--	ns
t11	Previous Data Valid after R/$\overline{C}$ Low	--	--	3.7	--	us
t7 + t8	Throughput Time	9, 10, 11	--	--	5	µs
t12[1]	R/$\overline{C}$ to $\overline{CS}$ Setup Time	9, 10, 11	10	--	--	ns
t13[1]	Time Between Conversions	9, 10, 11	5	--	--	µs
t14	Bus Access and Byte Delay	9, 10, 11	5	--	83	ns

1. Tested by application of signal at limit.
2. Internal timing specification, not directly measured.

FIGURE 1. CONVERSION TIMING WITH CS\ LOW

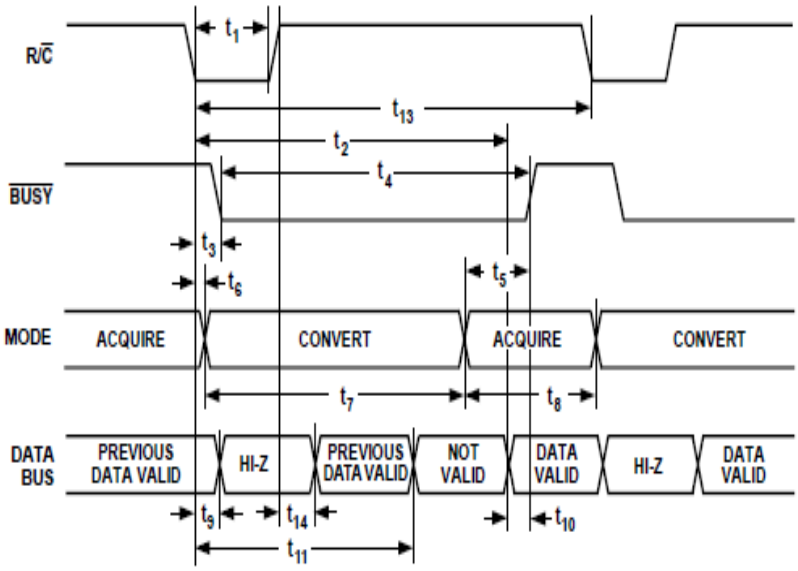


FIGURE 2. CS\ TO CONTROL CONVERSION & READ TIMING

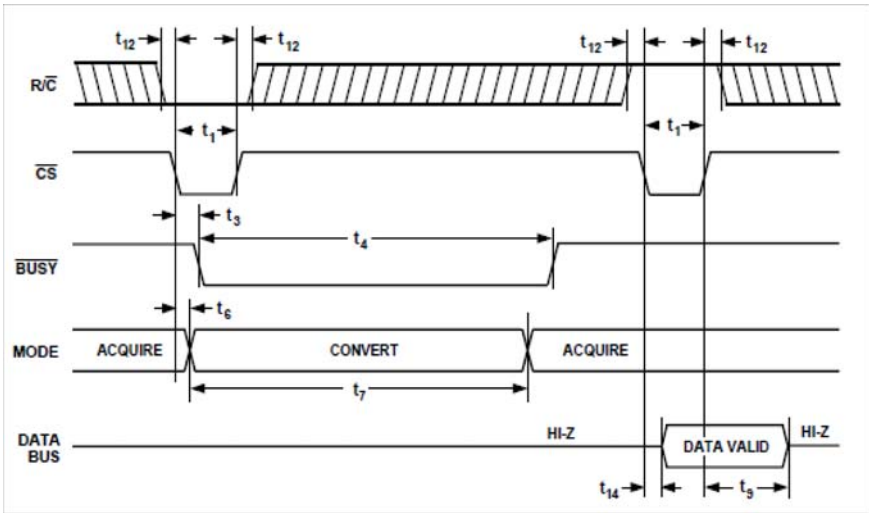
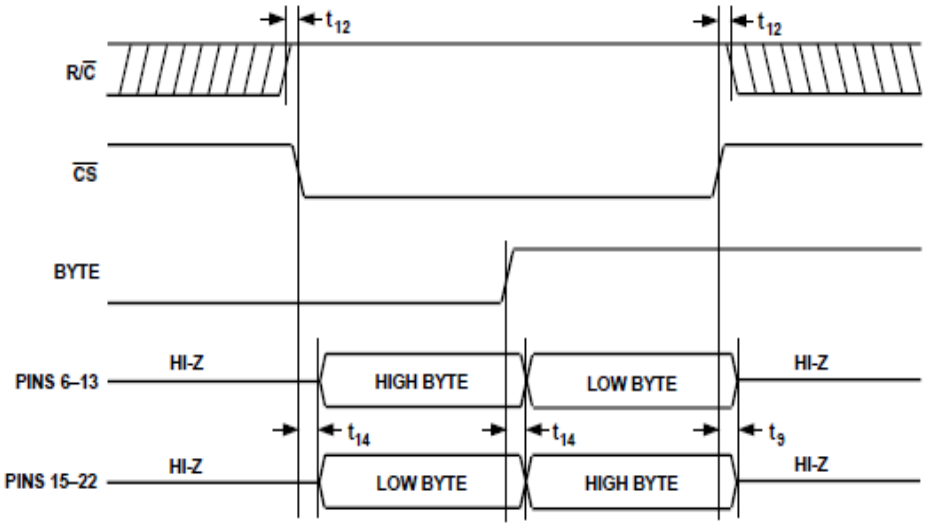
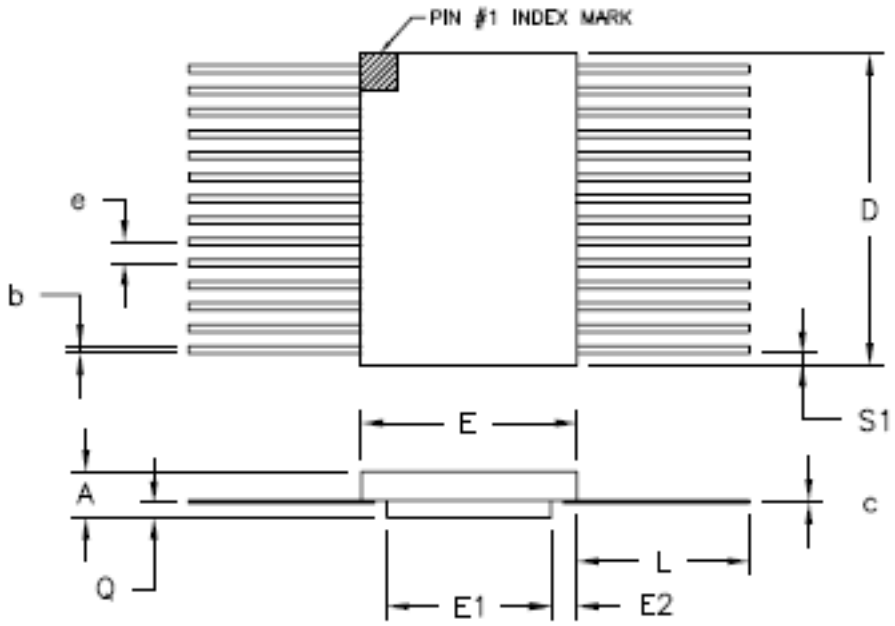


FIGURE 3. USING $\overline{CS}$ AND BYTE TO CONTROL DATA BUS READ TIMING





28-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.119	0.132	0.145
b	0.015	0.017	0.019
c	0.004	0.005	0.006
D	0,792	0.800	0.808
E	0.405	0.410	0.415
E1	0.245	0.250	0.255
E2	0.030	0.080	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.024	0.030	0.036
S1	0.020	0.067	--
N	28		

Note: All dimensions in inches
Top and Bottom of package internally connected to ground.

Important Notice:
These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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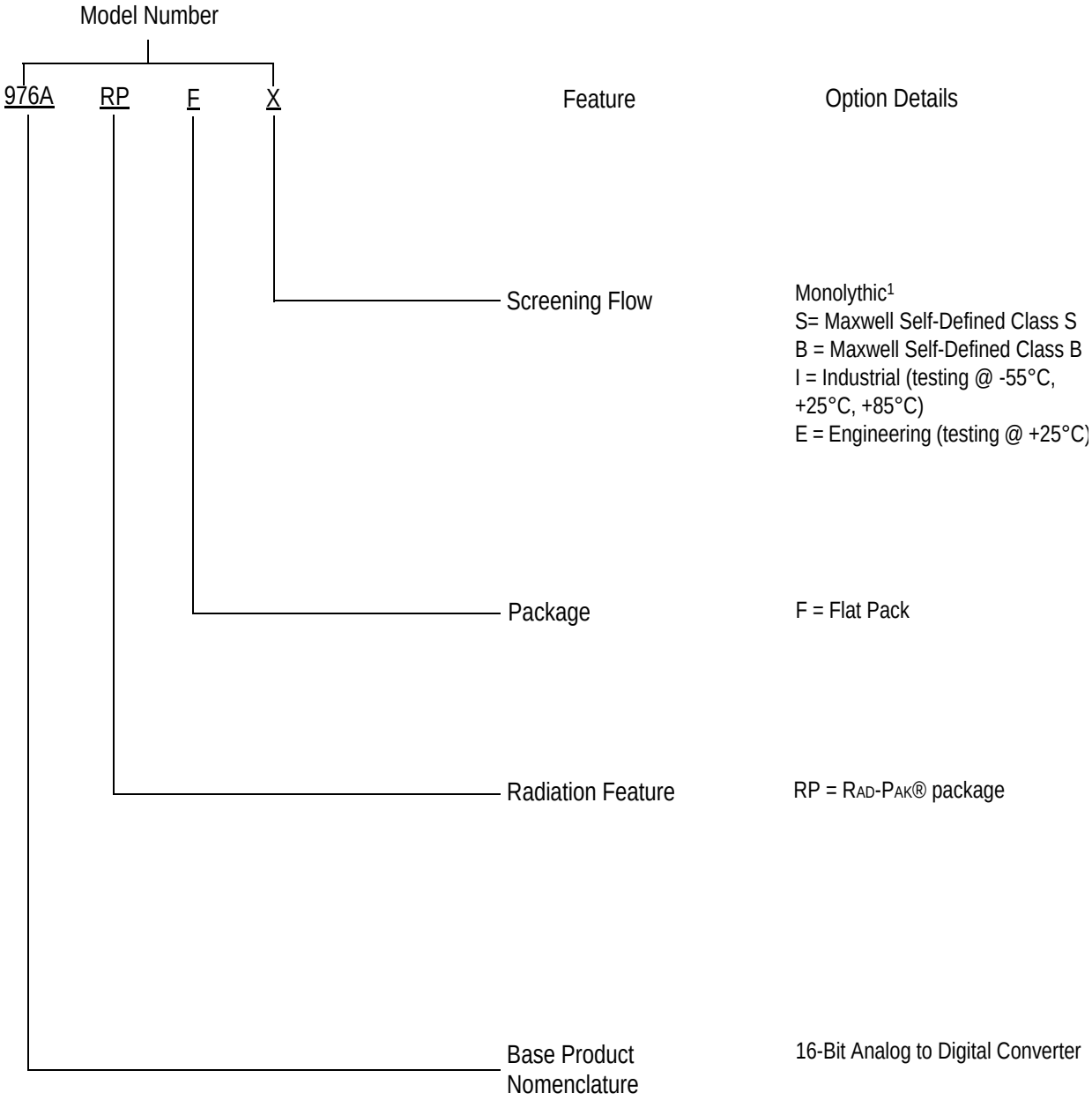
Product Ordering Options



1) Products are manufactured and screened to Maxwell Technologies self-defined Class B and Class S flows.