

IECQ

QC 88000-C004

COMPONENT

ISSUE 4

SPECIFICATION

May 2013

**Component Specification
For
Ceramic Hermetically Sealed
High Gain Photon Optocouplers**



M1077 IECQ

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FOREWORD

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The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognised Mark, or Certificate of Conformity. The components produced or services provided under the system are thereby acceptable in all member countries without further testing.

This Component Specification is based upon the requirements of IECQ 03-3, Annex E (QC 001002-2 Amendment 1, Clause 5.4) and has been prepared by:

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AMENDMENT RECORD

Issue 1 – Changed Page 4 – Amendments 10/09/09

Issue 2 – Changed Pages 3, 4, 5 & 6 – RoHS Compliant, Added CSM169-2 & Amendments 13/07/10

Issue 3 – Changed Page 6 – Added 4/5 pin hybrid outline drawing, changed page 5, changed description of 16 pin DIP, changed page 4, added solder dip options and amended level options 30/5/13

REQUIREMENTS

The requirements for IECQ Component Specifications as detailed in IECQ 03-3, Annex E (QC 001002-2 Amendment 1, Clause 5.4) are satisfied by the following data sheet.

It should note that IECQ are not responsible for manufacturers declarations made in data sheets which fall outside the limits of approved detailed in IECQ certificates.

This Component Specification is intended for use with applicable IECQ Assessment Specifications. Eg: QC 88000-A0001

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Ceramic Hermetically Sealed High Gain Photon Optocouplers

- | | |
|-------------|------------|
| ■ 6N134 | ■ CSM169-2 |
| ■ CD650/651 | ■ CSM169-4 |
| ■ CH350 | ■ CSM1600 |
| ■ CS600 | ■ MC600 |

Features

- Release to IECQ
- Hermetically Sealed
- High Density Packaging
- 1500V DC withstand Test Voltage
- Low Input Requirements
- High Current Transfer Ratio
- RoHS Compliant

Applications

- Military, high reliability system
- Medical instruments
- Mos, Cmos Applications
- Logic Interfacing
- Data Transmission
- Transportation

Description

Each channel contains a light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/ μ s. These optocouplers are for Isolation Voltage applications requiring up to 2500 Vdc.

The optocoupler family is also available in various package styles including 6, 8 and 16 pin DIP through hole, 16 pin surface mount DIP flat pack and a 6 Pin leadless ceramic chip carrier. The devices can be purchased with lead bend and plating options.

ISOCOM optocouplers are offered on the basis of similarity of emitter and detector therefore the performance characterization is identical, subject to the limitations of the packages. The wafer die similarities apply to the optocouplers for high reliability screening and radiation testing.

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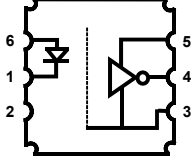
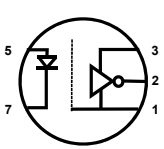

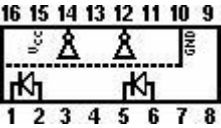
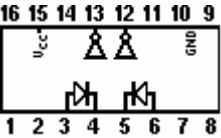
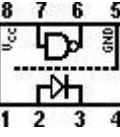
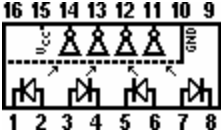
Selection Guide Package Styles and Configuration Options

Package	5 pin Hybrid	6 Pad LCC	6 pin Metal Can TO-5	8 pin DIP	16 pin DIP	16 pin Flat Pack
Lead Style						
Channels	1	1	1	1/2	2	2/4
Common Channel Wiring						

Isocom Part Numbers and Options

Commercial	CH350	CSM1600	MC600	CD650/651 CS600	6N134	CSM169
Defense Level	CH350/L2	CSM1600/L2	MC600/L2	CD650/651/L2 CS600/L2	6N134/L2	CSM169/L2
Space Level	CH350/L2S	CSM1600/L2S	MC600/L2S	CD650/651/L2S CS600/L2S	6N134/L2S	CSM169/L2S
Standard Gold Plate Finish		Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate
Solder Dipped		Option 20	Option 20	Option 20	Option 20	Option 20
Butt Cut/Gold Plate				Option 10	Option 10	
Gull Wing/Soldered				Option 30	Option 30	
Crew Cut/Gold Plate				Option 60	Option 60	

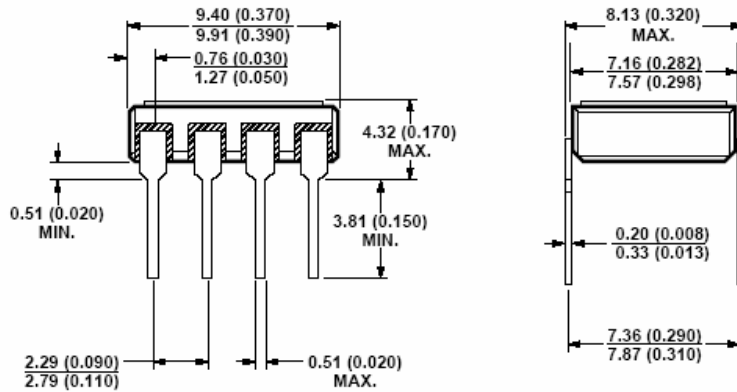
Functional Diagrams

CH350	CSM1600	MC600	CD650/651	6N134	CSM169-2
5 pin Hybrid	6 pad LCC	6 pin Metal Can	8 pin DIP	16 pin DIP	16 pin Flat Pack
1 Channel	1 Channel	1 Channel	2 Channel	2 Channel	2 Channel
					
			CS600		CSM169-4
			8 pin DIP		16 pin Flat Pack
			1 Channel		4 Channel
					

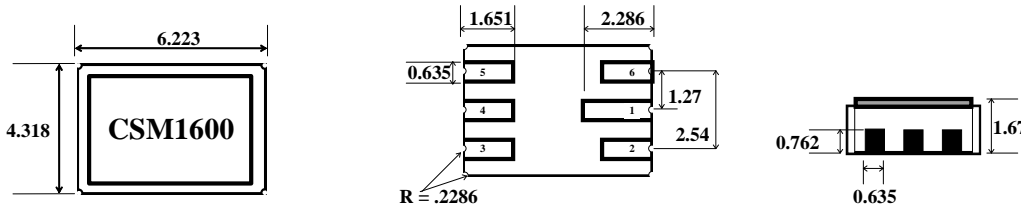
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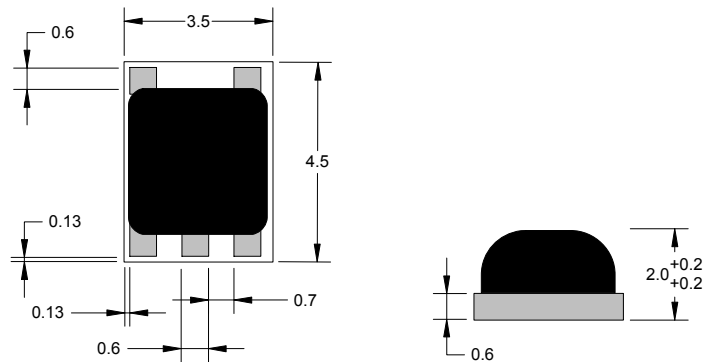
8 pin DIP 1 and 2 Channel



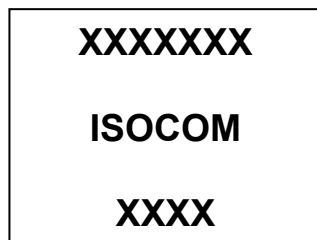
6 Terminal LCC Surface Mount, 1 Channel



4/5 Terminal Hybrid, 1 Channel



Device Marking

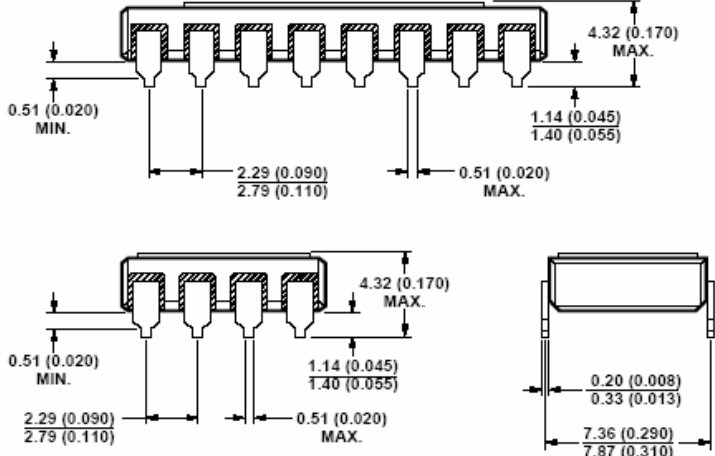
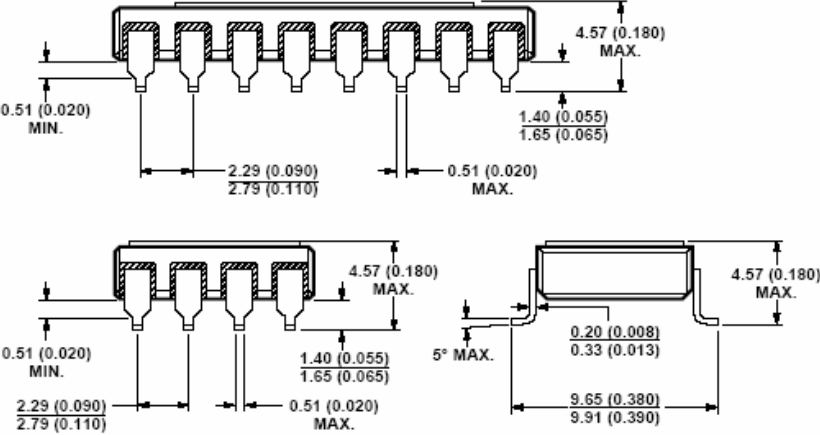
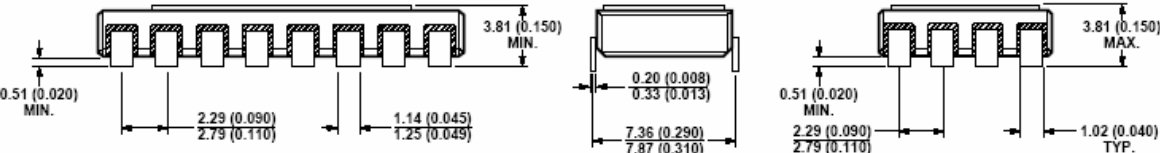


- ← Isocom Part Number
- ← Manufacturer
- ← Date Code (XX year XX week)

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Hermetic Optocoupler Options

Option	Description
10	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP</p> 
20	
30	<p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP.</p> 
60	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP</p> 

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Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C	
Operating Temperature	-55°C to +125°C	
Lead Soldering Temperature	260C for 10S, 1.6mm below seating plane where appropriate	

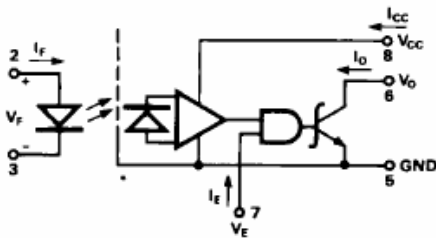
Input Diode

Peak Forward Current	40mA	$I_F (\leq 1 \text{ mS duration})$
Average Forward Current	20mA	I_F
Reverse Voltage	5V	V_R
Power Dissipation	35mW	

Output Detector

Supply Voltage	7V	V_{CC} (1minute maximum)
Current	25mA	I_O
Collector Power Dissipation	40mW	
Voltage	7V	V_O (See note 1)

Single Channel Schematic



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Electrical Characteristics

$T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ U.O.S.

All typical values at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$ (each channel where appropriate).

Parameter	Symbol	Test Conditions	Device	Min	Type	Max	Units
High Level Output Current (See note 1)	I_{OH}	$I_F = 250\mu\text{A}$, $V_O = V_{CC} = 5.5\text{V}$		-	20	250	μA
Lower Level Output Voltage (See notes 1 & 9)	V_{OL}	$I_F = 10\text{mA}$, $V_{CC} = 5.5\text{V}$, $I_{OL}(\text{sinking}) = 10\text{mA}$		-	0.4	0.6	V
		$I_F = 5\text{mA}$, $V_{CC} = 5.5\text{V}$, $I_{OL}(\text{sinking}) = 13\text{mA}$	CD650				
High Level Supply Current	I_{CCH}	$V_{CC} = 5.5\text{V}$, $I_{F1} = I_{F2} = 0$		-	15	30	mA
Low Level Supply Current	I_{CCL}	$V_{CC} = 5.5\text{V}$, $I_{F1} = I_{F2} = 10\text{mA}$	CS600	-	15	19	mA
			CD650 CD651		20	38	
		$V_{CC} = 5.5\text{V}$, $I_{F1} = I_{F2} = 13\text{mA}$	CH350			36	
		$V_{CC} = 5.5\text{V}$, $I_{F1} = I_{F2} = 20\text{mA}$	6N134			36	
Input-Output Insulation Leakage Current (See notes 2 & 10)	I_{LO}	RH = 45%, $T_A = 25^{\circ}\text{C}$, $t = 5\text{S}$ $V_{IO} = 1500\text{Vdc}$		-	-	1.0	μA
Input Forward Voltage (See note 1)	V_F	$I_F = 10\text{mA}$, $T_A = 25^{\circ}\text{C}$		-	1.5	1.9	V
		$I_F = 20\text{mA}$		-	-	1.9	
Input Reverse Breakdown Voltage (See note 1)	B_{VR}	$I_R = 10\mu\text{A}$, $T_A = 25^{\circ}\text{C}$		5	-	-	V
Propagation Delay Time to High Output Level See notes 1 & 5)	t_{PLH}	$R_L = 510\Omega$, $I_F = 13\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$	6N134	-	-	100	nS
		$R_L = 510\Omega$, $I_F = 13\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 15\text{pF}$	6N134 CD651	-	60	90	
			CH350			200	
		$R_L = 350\Omega$, $I_F = 7.5\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 15\text{pF}$	CS600			75	
Propagation Delay Time to Low Output Level (See notes 1 & 6)	t_{PHL}	$R_L = 510\Omega$, $I_F = 13\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$	6N134	-	-	100	nS
		$R_L = 510\Omega$, $I_F = 13\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 15\text{pF}$	6N134 CD651	-	55	90	
		$R_L = 510\Omega$, $I_F = 13\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 15\text{pF}$	CH350			200	
		$R_L = 350\Omega$, $I_F = 7.5\text{mA}$, $T_A = 25^{\circ}\text{C}$, $C_L = 15\text{pF}$	CS600 CD650			100	
Current Transfer Ratio (See note 1)	CTR	$I_F = 10\text{mA}$, $V_O = 0.6\text{V}$, $V_{CC} = 5.5\text{V}$		100	-	-	%
		$I_F = 5\text{mA}$, $V_O = 0.6\text{V}$, $V_{CC} = 5.5\text{V}$	CS600 CD650	100	300		

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Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$ each channel where appropriate

Parameter	Symbol	Test Conditions	Notes	Min	Type	Max	Units
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	$I_F = 20\text{mA}$	1	-	-1.9	-	mV/°C
Resistance	R_{I-O}	$V_{I0} = 500\text{V}$	3	-	10^{12}	-	Ω
Capacitance	C_{I-O}	$f = 1\text{MHz}$	3	-	1.9	-	pF
Input Capacitance	C_{IN}	$f = 1\text{MHz}$, $V_F = 0$	1	-	60	-	pF
Input-Input Leakage Current	I_{I-I}	45% Relative Humidity $V_{II} = 500\text{Vdc}$, $t = 5\text{S}$	4	-	0.5	-	nA
Resistance	R_{I-I}	$V_{II} = 500\text{Vdc}$	4	-	10^{12}	-	Ω
Capacitance	C_{I-I}	$f = 1\text{MHz}$	4	-	0.6	-	pF
Output Rise (10-90%)	tr	$R_L = 510\Omega$, $C_L = 15\text{pF}$, $I_F = 13\text{mA}$	1	-	35	-	nS
Output Fall Time (90-10%)	tf	$R_L = 510\Omega$, $C_L = 15\text{pF}$, $I_F = 13\text{mA}$	1	-	35	-	nS
Common Mode Transient Immunity at Logic High Output Level	CM_H	$V_O(\text{min}) = 2\text{V}$, $V_{CM} = 10\text{V (peak)}$ $R_L = 510\Omega$, $I_F = 0\text{mA}$	1 & 7	-	1000	-	V/ μS
Common Mode Transient Immunity at Logic Low Output Level	CM_L	$V_O(\text{max}) = 0.8\text{V}$, $V_{CM} = 10\text{V (peak)}$ $R_L = 510\Omega$, $I_F = 10\text{mA}$	1 & 8	-	-1000	-	V/ μS

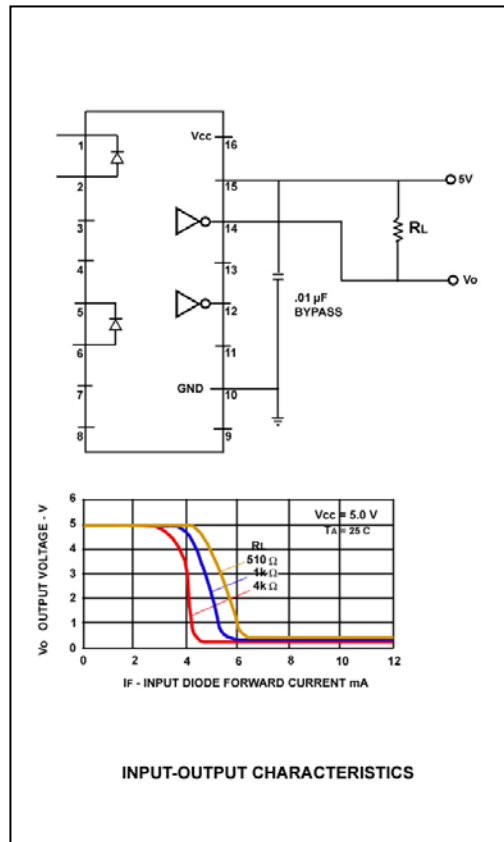
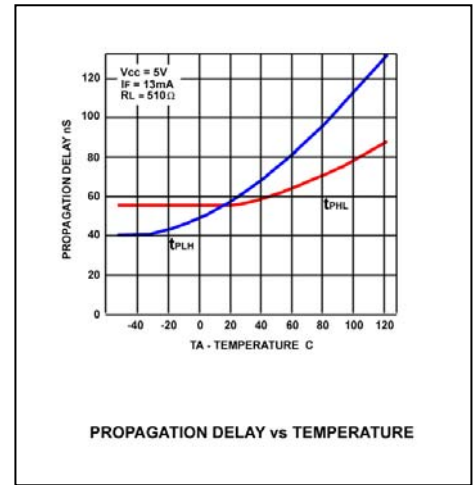
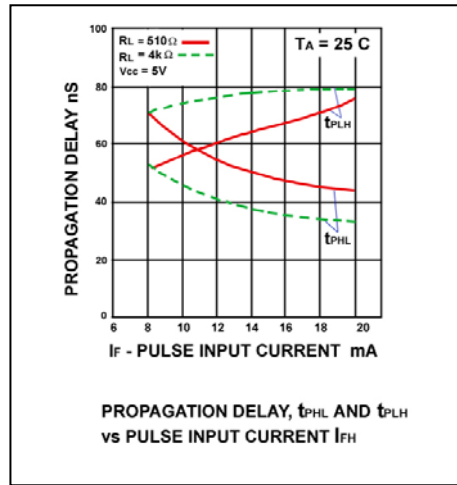
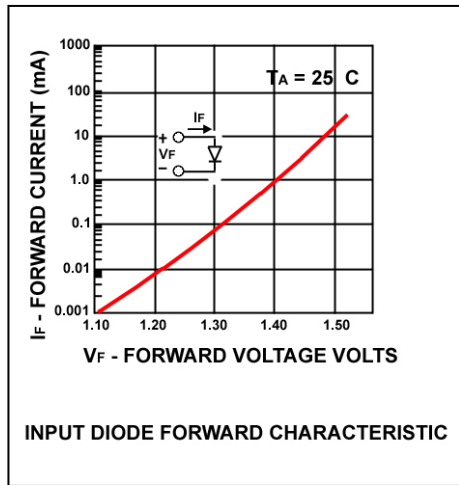
Notes: (Apply typically to 16 pin package)

1. Each channel, where appropriate.
2. Measured between pins 1 through 4 shorted together, and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2, or 5 and 6 shorted together, and pins 9 through 16 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., $V_O > 2.0\text{V}$).
8. CM_L is the maximum tolerable common mode transient to assure that the output will remain in the logic low state (i.e., $V_O < 2.0\text{V}$).
9. It is essential that a bypass capacitor (0.1 to 0.1 μF , ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm.
10. This is a momentary withstand test, not an operating condition.

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