69F64G16
69F128G16
69F256G16
64 Gb, 128 Gb, 256 Gb x16
NAND Flash Module

Preliminary

FEATURES:

NAND Flash Interface
- Single Level Cell (SLC) Technology
- ONFI 2.2 Compliant

Operating Voltage
- VCC 3.0 - 3.6V
- VCCQ 1.7 - 1.95V or 3.0-3.6V

High density
- 32Gbit per FLASH NAND die
- Supports higher speed designs with less capacitance/fewer I/O's to drive

Page Size
- 8640 bytes (8192 + 448 spare bytes)
- Supports external BCH correction algorithms (16 bit correction per 540 bytes)

Features
- High reliability data storage for demanding space applications
- Ceramic hermetic package with built-in TID shielding
- Two separate isolated FLASH memory banks (isolated control, data and power)
  - Can be used separately or tied together on customer board
- Class E, I, H or K
- 64G16, 128G16 and 256G16 densities with same footprint/pinout functionality

Speed
- Can be used in asynch or synch mode
- Asynch: Up to asynch timing mode 5 (50MT/sec)
- Synch: Up to synchronous timing mode 5 (200MT/sec)

Temperature Range
- -55°C to 125°C

Endurance
- 60,000 cycles

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Supported Features
ONFI 1.0, 2.0, 2.1, 2.2
Interleaved (multi-plane) operations
Multiple LUN operations
Small Data Move
Interleaved Address restrictions for cache operations
No interleaved block address restrictions
Overlapped/concurrent interleaving supported
Supports timing modes: 0 thru 5
Supports driver strength settings: underdrive, overdrive 1 and 2

Supported Commands:
Reset
Synchronous Reset
Reset LUN
Get Features
Set Features
Read Status
Read Status Enchanced
Change Row Address
Read Mode
Read Page Interleaved
Read Page Cache Sequential
Read Page Cache Random
Read Page Cache Last
Program Page
Program Page Interleaved
Program Page Cache
Erase Block
Erase Block Interleaved
Copyback Read
Copyback Program
Copyback Program Interleaved
Read Unique ID
Read Parameter Page
Read ID

Not Supported
Non-sequential page programming
16 bit data bus width per Target/LUN
Extended ECC

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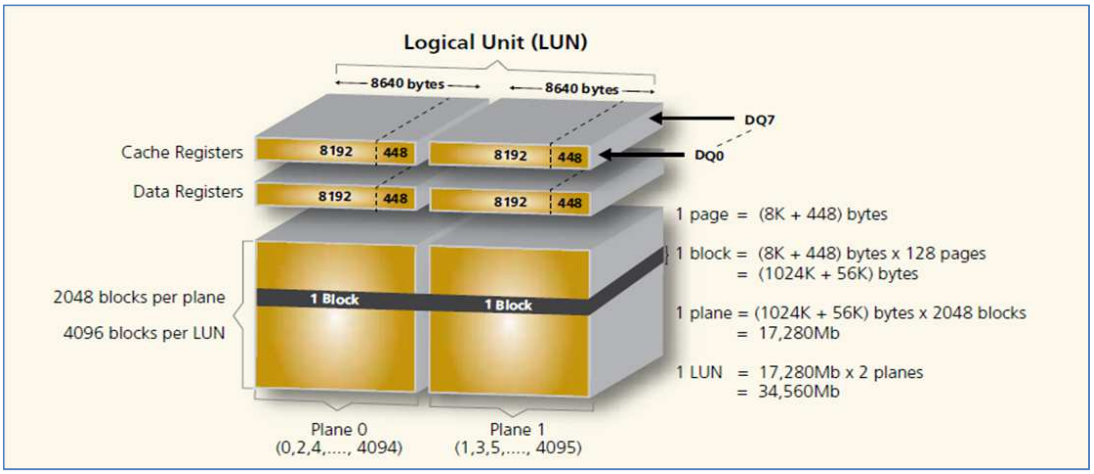
Array Organization



Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	L	L	L	L	LUN	BA18	BA17	BA16

CA[n] = Column Address
PA[n] = Page Address
BA[n] = Bank Address
LUN = Logical Unit Address
Row Address = LUN, Bank, Page Address
BA[7] = Plane select
Column Addresses above 8639 are invalid (page size = 8192 + 448)

Memory Organizatoin
Bytes per page: 8192
Spare ECC bytes per page: 448
Pages per block: 128
Blocks per LUN: 4096
LUNs per chip enable: 2; 64G16 is 1 LUN per chip enable
Column address cycles: 2
Row address cycles: 3
Bits per cell: 1
Bad blocks maximum per LUN: 80
Block endurance: 60,000
Programs per page: 4
Number of interleave address bits: 1

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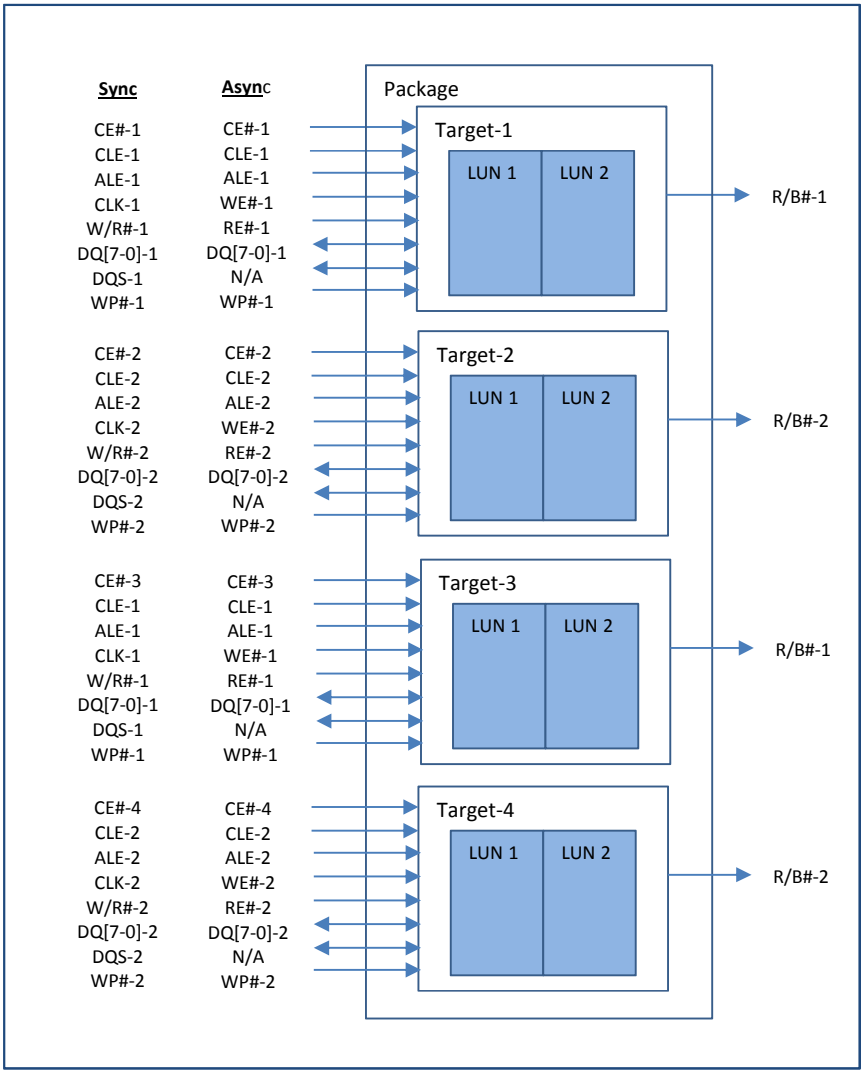
Package Organization 69F256G16



Architecture
Independent 8 bit buses per package: 2
Targets per 8 bit bus: 2
LUNS per Target: 2
(4 die per 8 bit bus)
(8 die per package)

DQ[7-0]-1	CE-1#, CE-3#
	RB-1#
	RE-1#, WR-1#
	CLE-1, ALE-1
	WE-1#/CLK-1
	WP-1#, DQS-1

DQ[7-0]-2	CE-2#, CE-4#
	RB-2#
	RE-2#, WR-2#
	WE-2#/CLK-2
	WP-2#, DQS-2

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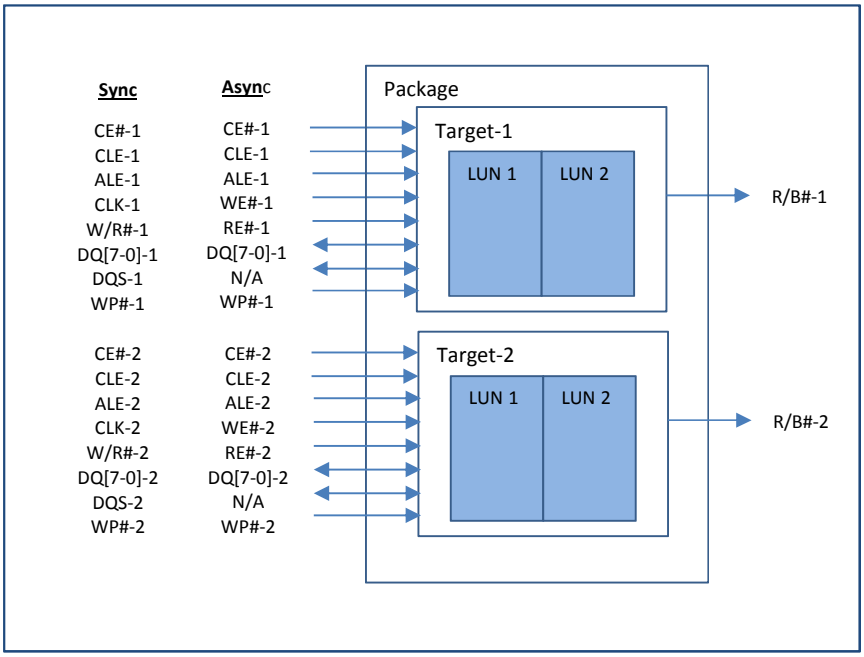
Package Organization 69F128G16



Architecture
Independent 8 bit buses per package: 2
Targets per 8 bit bus: 1
LUNS per Target: 2
(2 die per 8 bit bus)
(4 die per package)

DQ[7-0]-1	CE-1#
	RB-1#
	RE-1#, WR-1#
	CLE-1, ALE-1
	WE-1#/CLK-1
	WP-1#, DQS-1

DQ[7-0]-2	CE-2#
	RB-2#
	RE-2#, WR-2#
	WE-2#/CLK-2
	WP-2#, DQS-2

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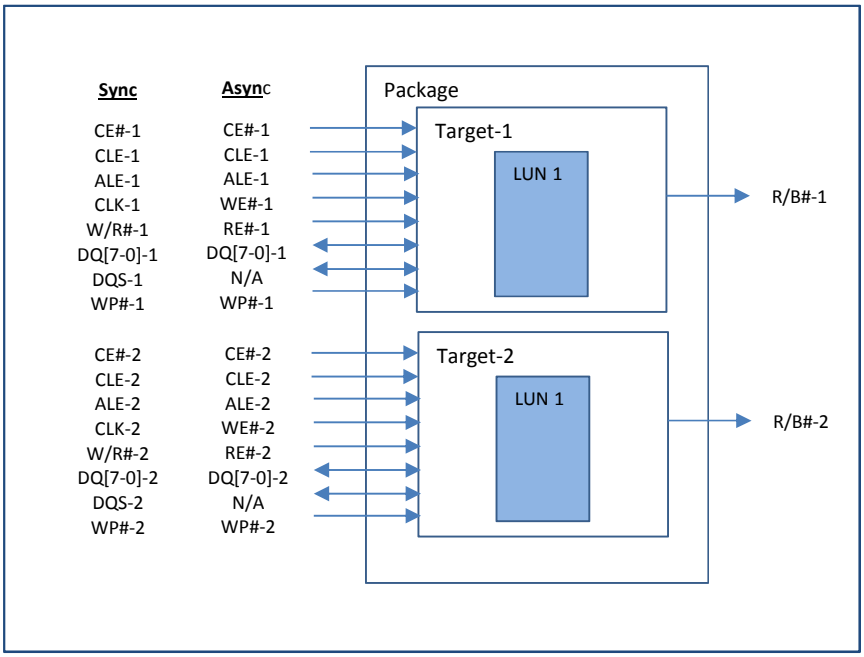
Package Organization 69F64G16



Architecture
Independent 8 bit buses per package: 2
Targets per 8 bit bus: 1
LUNS per Target: 1
(1 die per 8 bit bus)
(2 die per package)

DQ[7-0]-1	CE-1#
	RB-1#
	RE-1#, WR-1#
	CLE-1, ALE-1
	WE-1#/CLK-1
	WP-1#, DQS-1

DQ[7-0]-2	CE-2#
	RB-2#
	RE-2#, WR-2#
	WE-2#/CLK-2
	WP-2#, DQS-2

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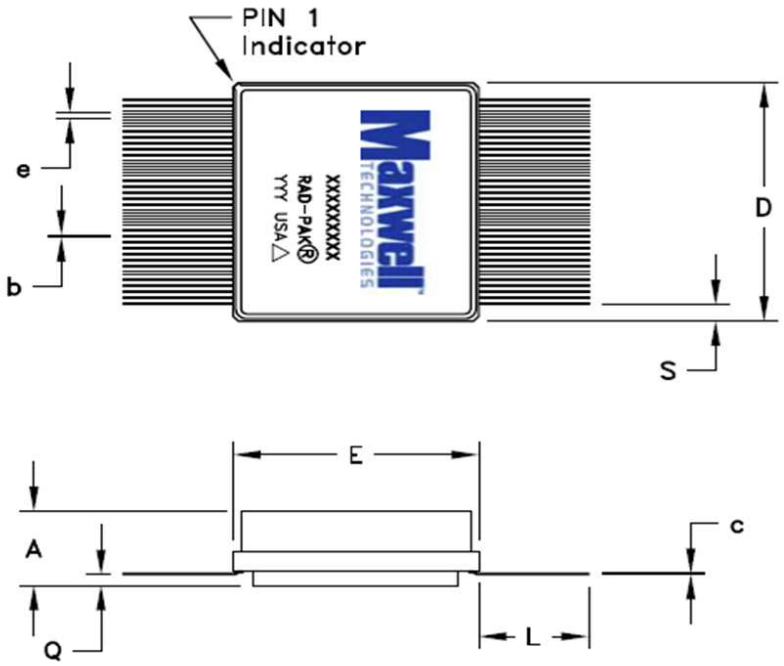

68 LEAD FLAT PACKAGE			
	DIMENSION		
SYMBOL	MIN	NOM	MAX
A	0.241	0.260	0.279
b	0.006	0.008	0.010
c	0.005	0.006	0.007
D	0.985	1.000	1.015
e	0.025 BSC		
E	0.810	0.82	0.830
L	0.390	0.400	0.410
Q	0.014	0.021	0.029
S	0.064	0.084	0.104
NOTE: ALL DIMENSIONS IN INCHES			

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Pinout[1]

64G16 & 128G16	256G16				256G16	64G16 & 128G16
Pin Description	**Pin Description**	**Pin #**		**Pin #**	**Pin Description**	**Pin Description**
same	VSS	1		68		same
same	VCC-1	2		67	VCC-2	same
same	WP#-1	3		66	WP#-2	same
same	WE#/CLK-1	4		65	WE#/CLK-2	same
same	ALE-1	5		64	ALE-2	same
same	CLE-1	6		63	CLE-2	same
NC[2]	CE#3	7		62	CE#4	NC[2]
same	CE#1	8		61	CE#2	same
same	RE#/WR#-1	9		60	RE#/WR#-2	same
same	RB#-1	10		59	RB#-2	same
same	VSS	11		58	VSS	same
same	VCC-1	12		57	VCC-2	same
same	VSS	13		56	VSS	same
same	VSSQ	14		55	VSSQ	same
same	VCCQ-1	15		54	VCCQ-2	same
same	DQ7-1	16		53	DQ7-2	same
same	DQ6-1	17		52	DQ6-2	same
same	DQ5-1	18		51	DQ5-2	same
same	DQ4-1	19		50	DQ4-2	same
same	VSSQ	20		49	VSSQ	same
same	VCCQ-1	21		48	VCCQ-2	same
same	VCC-1	22		47	VCC-2	same
same	VSS	23		46	VSS	same
same	DQS-1	24		45	DQS-2	same
same	VCCQ-1	25		44	VCCQ-2	same
same	VSSQ	26		43	VSSQ	same
same	DQ3-1	27		42	DQ3-2	same
same	DQ2-1	28		41	DQ2-2	same
same	DQ1-1	29		40	DQ1-2	same
same	DQ0-1	30		39	DQ0-2	same
same	VCCQ-1	31		38	VCCQ-2	same
same	VSSQ	32		37	VSSQ	same
same	VSS	33		36	VSS	same
same	VCC-1	34		35	VCC-2	same

1. Two independent 8 bit buses; Bus-1 and Bus-2 completely isolated (DQ, control, Power)
2. NC = Not internally connected

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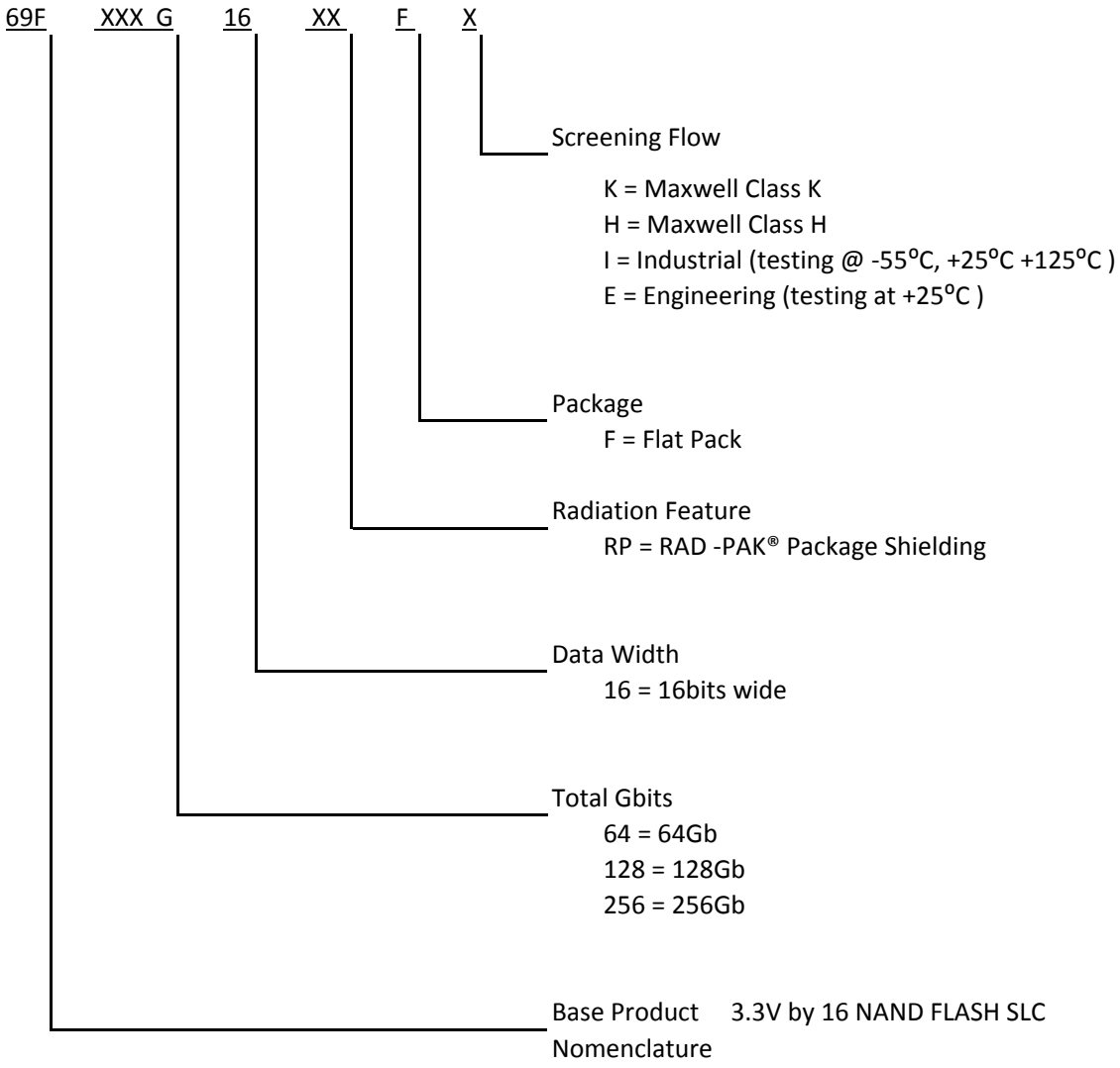
Product Ordering Options



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