NAND Flash Module
69F12G24, 69F24G24, 69F96G24, 69F192G24

Preliminary

FEATURES: 69F12Gb, 69F24Gb (4Gb die)

High density
- 4Gbit per FLASH NAND die
- Supports higher speed designs with less capacitance/fewer I/O's to drive

NAND Flash Interface
- Single Level Cell (SLC) Technology
- ONFI 1.0 Compliant

Operating Voltage
- VCC 3.0 - 3.6V

Page Size
- 2112 bytes (2048 + 64 spare bytes)
- Includes internal BCH correction algorithms (4 bit correction per 528 bytes)

Features
- High reliability data storage for demanding space applications
- Ceramic hermetic package with built-in TID shielding
- Three separate FLASH memory banks, supports TMR error correction
- Class E, I, H or K

Speed
- Asynch: Up to asynch timing mode 5 (50MT/sec)

Temperature Range
- -55°C to 125°C

Endurance
- 100,000 cycles

FEATURES: 69F 96Gb, 69F192Gb (32Gb die)

High density
- 32Gbit per FLASH NAND die
- Supports higher speed designs with less capacitance/fewer I/O's

NAND Flash Interface
- Single Level Cell (SLC) Technology
- ONFI 2.2 Compliant

Operating Voltage
- VCC 3.0 - 3.6V
- VCCQ 1.7 - 1.95V or 3.0-3.6V

Page Size
- 8640 bytes (8192 + 448 spare
- Supports external BCH correction algorithms (up to 16 bit correction per 540 bytes)

Features
- High reliability data storage for demanding space applications
- Ceramic hermetic package with built-in TID shielding
- Three separate FLASH memory banks, supports TMR error
- Class E, I, H or K

Speed
- Asynch: Up to asynch timing mode 5 (50MT/sec)
- Synch: Up to synchronous timing mode 5 (200MT/sec)

Temperature Range
- -55°C to 125°C

Endurance
- 60,000 cycles

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Supported Commands:	4Gb die		32Gb die	
Reset	FFh	-	FFh	-
Synchronous Reset			FCh	-
Reset LUN			FAh	-
Get Features	EEh	-	EEh	-
Set Features	EFh	-	EFh	-
Read Status	70h	-	70h	-
Read Status Enchanced (Multi-LUN)	78h	-	78h	-
Change Read Column (Random data output)	05h	E0h	05h	E0h
Change Read Column Enhanced	06h	E0h	06h	E0h
Change Write Column (Random data input)	85h	-	85h	-
Change Row Address			85h	-
Read Mode	00h	-	00h	-
Read Page	00h	30h	00h	30h
Read Page Interleaved	00h	00h, 30h	00h	32h
Read Page Cache Sequential *	31h	-	31h	-
Read Page Cache Random *	00h	31h	00h	31h
Read Page Cache Last *	3Fh	-	3Fh	-
Program Page	80h	10h	80h	10h
Program Page Interleaved	80h	11h-85h,10h	80h	11h
Program Page Cache *	80h	15h	80h	15h
Erase Block	60h	D0h	60h	D0h
Erase Block Interleaved	60h	D1h	60h	D1h
Copyback Read	00h	35h	00h	35h
Copyback Program	85h	10h	85h	10h
Copyback Program Interleaved	85h	11h	85h	11h
Read Unique ID	EDh	-	EDh	-
Read Parameter Page	ECh	-	ECh	-
Read ID	90h	-	90h	-

* These commands supported with internal ECC disabled

Not Supported
Non-sequential page programming
16 bit data bus width per Target/LUN
Extended ECC
Synchronous Mode: clock stopped for data input

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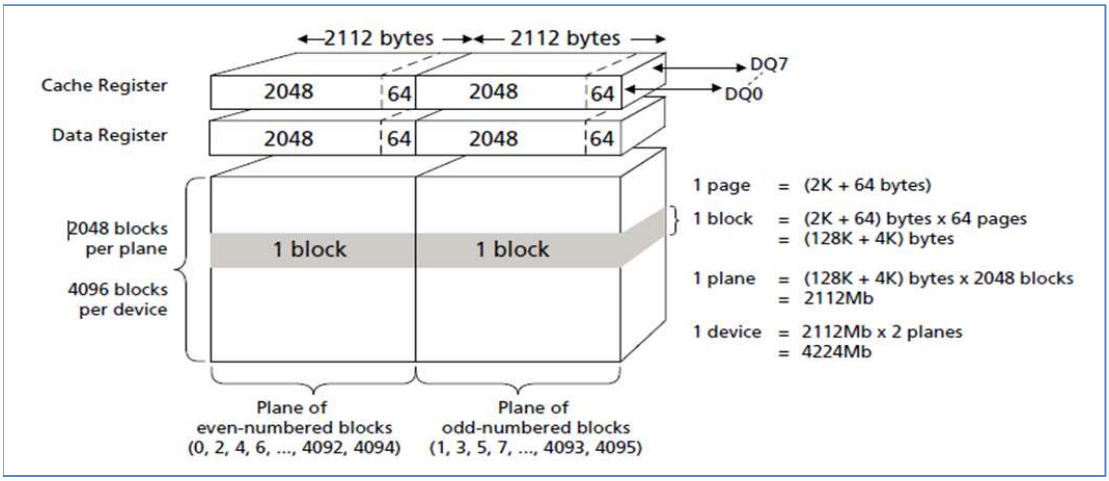
Array Organization: 4Gb Die



Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	L	L	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	L	L	L	L	L	LUN/BA18	BA17	BA16

CA[n] = Column Address
PA[n] = Page Address
BA[n] = Bank Address
LUN = Logical Unit Address
Row Address = LUN, Bank, Page Address
BA[6] = Plane Select
Column Addresses above 2111 are invalid (page size =2048 + 64)

Memory Organization
Bytes per page: 2048
Spare ECC bytes per page: 64
Pages per block: 64
Blocks per LUN: 4096
LUNs per chip enable: 2
Column address cycles: 2
Row address cycles: 3
Bits per cell: 1
Bad blocks maximum per LUN: 80
Block endurance: 100,000
Programs per page: 4
Number of bits ECC required: 1 (for 512 Bytes)
Number of interleave address bits: ?

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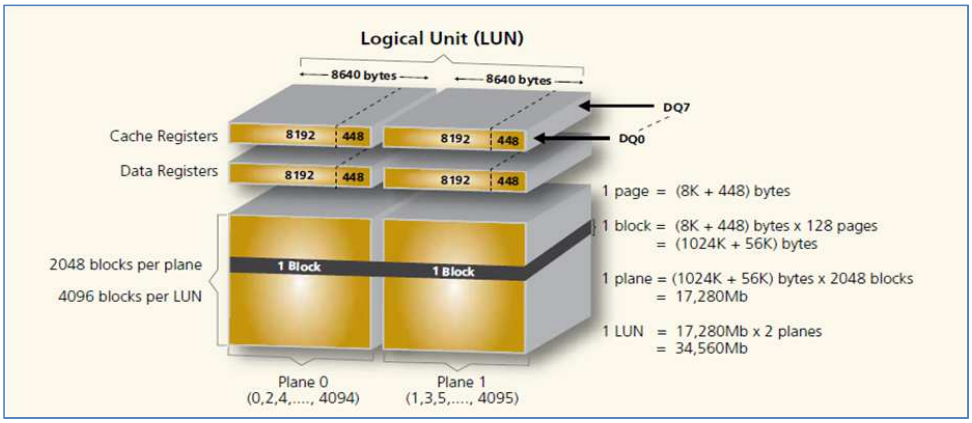
Array Organization: 32Gb Die

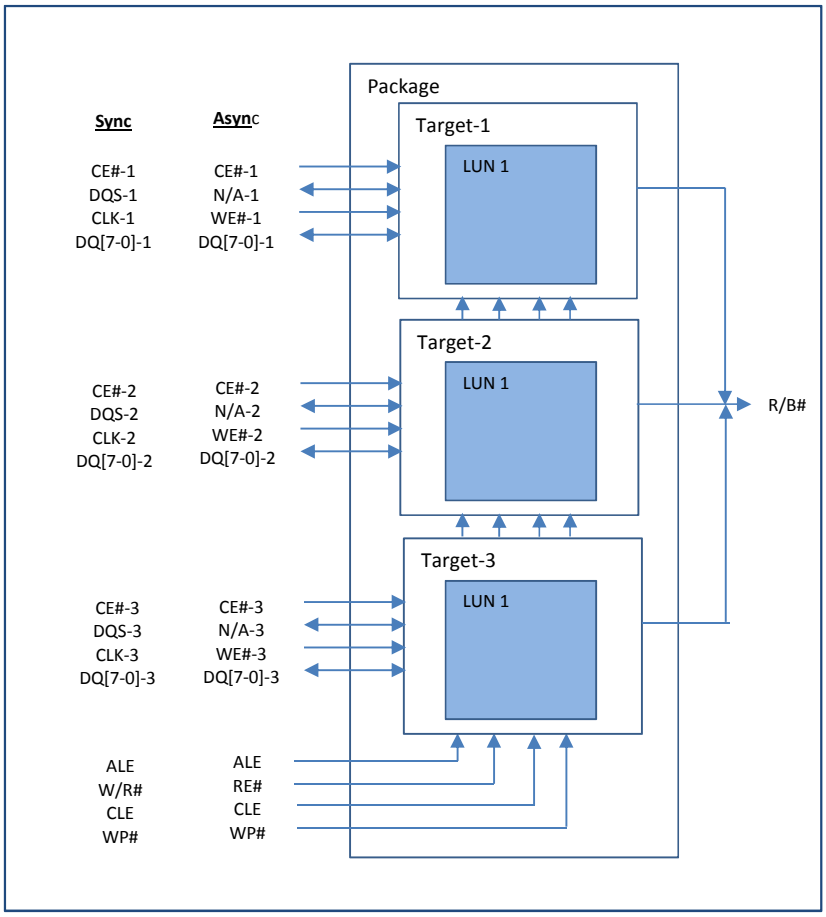


Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	L	L	L	L	LUN	BA18	BA17	BA16

CA[n] = Column Address
PA[n] = Page Address
BA[n] = Bank Address
LUN = Logical Unit Address
Row Address = LUN, Bank, Page Address
BA[7] = Plane select
Column Addresses above 8639 are invalid (page size = 8192 + 448)

Memory Organization
Bytes per page: 8192
Spare ECC bytes per page: 448
Pages per block: 128
Blocks per LUN: 4096
LUNs per chip enable: 2
Column address cycles: 2
Row address cycles: 3
Bits per cell: 1
Bad blocks maximum per LUN: 80
Block endurance: 60,000
Programs per page: 4
Number of bits ECC required: 8 (for 512 Bytes)
Number of interleave address bits: 1

Package Organization 12Gb X 24
96Gb X 24



Architecture
Independent 8 bit buses per package: 3
Targets per 8 bit bus: 1
LUNS per Target:
(1 die per 8 bit bus)
(3 die per package)

DQ[7-0]-1	CE#-1
	WE-1#/CLK-1
	DQS-1

DQ[7-0]-2	CE#-2
	WE#-2/CLK-2
	DQS-2

DQ[7-0]-3	CE#-3
	WE#-3/CLK-3
	DQS-3

Shared	ALE
	RE#, W/R#
	CLE
	WP#
	RB#

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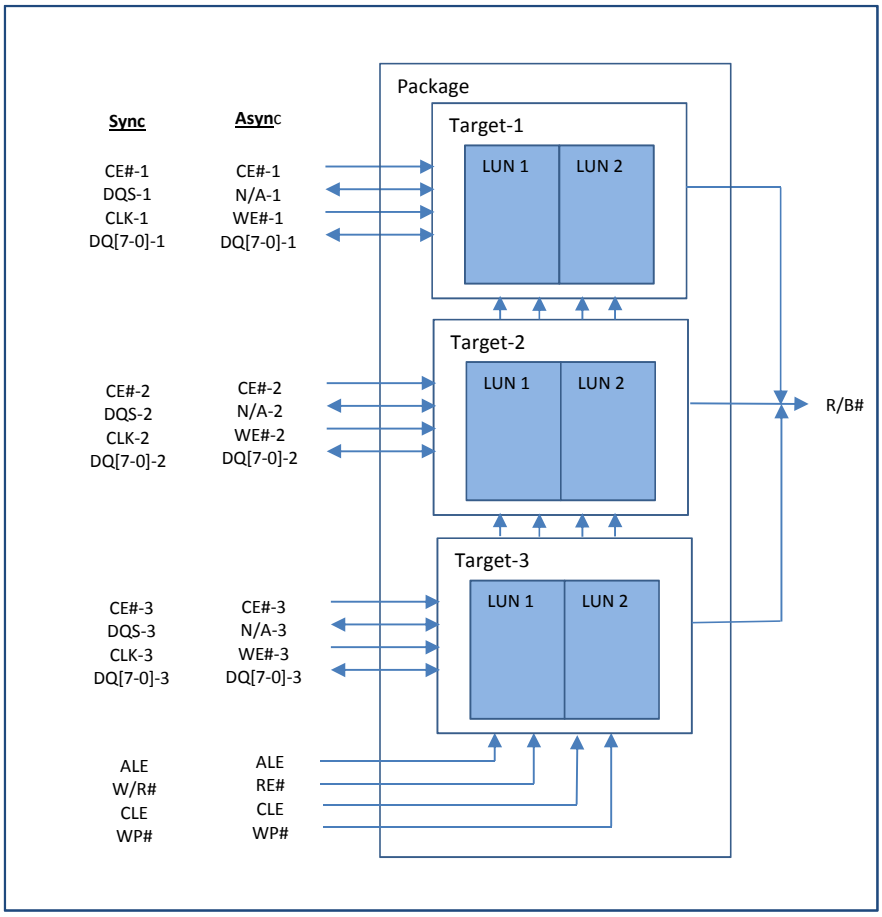
Package Organization 24Gb X 24
192Gb X 24



Architecture
Independent 8 bit buses per package: 3
Targets per 8 bit bus: 1
LUNS per Target: 2
(2 die per 8 bit bus)
(6 die per package)

DQ[7-0]-1	CE#-1
	WE-1#/CLK-1
	DQS-1

DQ[7-0]-2	CE#-2
	WE#-2/CLK-2
	DQS-2

DQ[7-0]-3	CE#-3
	WE#-3/CLK-3
	DQS-3

Shared	ALE
	RE#, W/R#
	CLE
	WP#
	RB#

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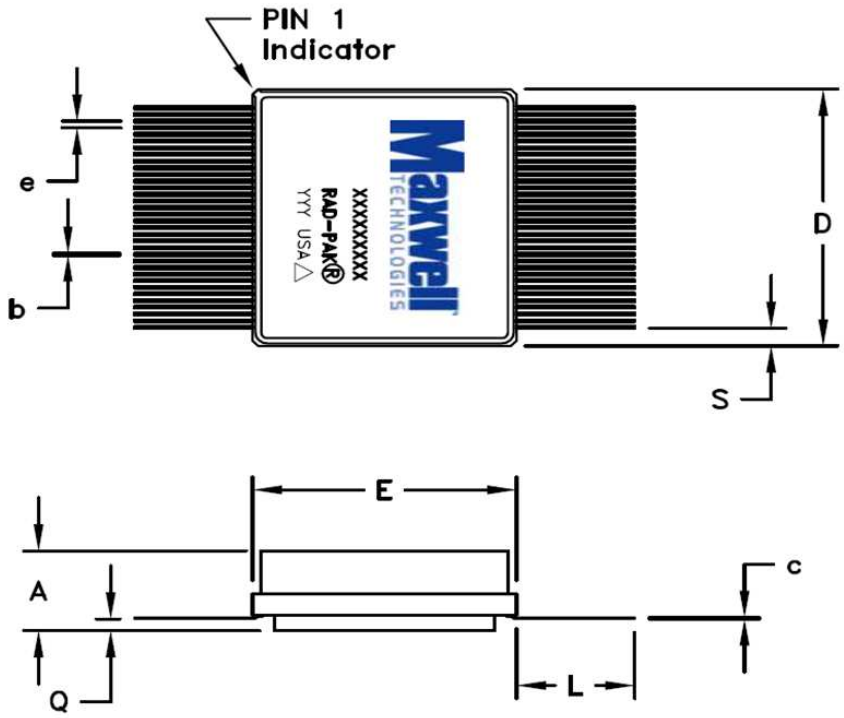

	DIMENSION		
SYMBOL	MIN	NOM	MAX
A	0.241	0.260	0.279
b	0.006	0.008	0.010
c	0.005	0.006	0.007
D	0.985	1.000	1.015
e		0.025 BSC	
E	0.810	0.820	0.830
L	0.390	0.400	0.410
Q	0.014	0.021	0.029
S	0.051	0.071	0.091

NOTE: ALL DIMENSIONS IN INCHES

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Pinout

Description	Description	Pin #	Pin #	Description	Description
4Gb die Differences	32Gb die Aysnc/Sync			32Gb die Aysnc/Sync	4Gb die Differences
→	VCC	1	70	VCCQ	VCC
→	VSS	2	69	VSSQ	VSS
→	CLE	3	68	DQ16	←
→	CE#-1	4	67	DQ17	←
→	CE#-2	5	66	DQ18	←
→	CE#-3	6	65	DQ19	←
→	VCC	7	64	VCCQ	VCC
→	VSS	8	63	VSSQ	VSS
WE#-1	WE# / CLK-1	9	62	DQ20	←
→	RB#	10	61	DQ21	←
WE#-2	WE# / CLK-2	11	60	DQ22	←
VCC	VCCQ	12	59	DQ23	←
VSS	VSSQ	13	58	VCCQ	VCC
WE#-3	WE# / CLK-3	14	57	VSSQ	VSS
RE#	RE#/W/R#	15	56	DNU / DQS-3	NC
→	ALE	16	55	VCC	←
→	VCC	17	54	VSS	←
→	VSS	18	53	WP#	←
DNC	DNU / DQS-1	19	52	DNU / DQS-2	NC
VCC	VCCQ	20	51	VCCQ	VCC
VSS	VSSQ	21	50	VSSQ	VSS
→	DQ7	22	49	DQ15	←
→	DQ6	23	48	DQ14	←
→	DQ5	24	47	DQ13	←
→	DQ4	25	46	DQ12	←
VCC	VCCQ	26	45	VCCQ	VCC
VSS	VSSQ	27	44	VSSQ	VSS
→	DQ3	28	43	DQ11	←
→	DQ2	29	42	DQ10	←
→	DQ1	30	41	DQ9	←
→	DQ0	31	40	DQ8	←
VCC	VCCQ	32	39	VCCQ	VCC
VSS	VSSQ	33	38	VSSQ	VSS
→	VCC	34	37	VCC	←
→	VSS	35	36	VSS	←

Three 8 bit buses; Each with its own CS[0-2], DQS[0-2] & WE#CLK[0-2]
Three chip selects for 6 die using Multi-LUN operation.
All other control signals are shared; CLE, RB#, RE#-W/R#,ALE & WP#
Arrow indicates the same signal between die types
VCCQ and VSSQ are not separated from VCC and VSS for 4Gb die

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Feature Summary

Description	4Gb die	32Gb die
ONFI 1.0, 2.0, 2.1, 2.2	1.0	1.0 to 2.2
Program page register clear enhancement		Yes
Extended parameter page		No
Interleaved read operations	Yes	Yes
Synchronous interface		Yes
Odd to even page copyback	Yes	Yes
Interleaved Porgram and erase operations	Yes	Yes
Non-sequential page programming	No	No
Multiple LUN operations	Yes	Yes
16 bit data bus width per LUN	No	No
RESET LUN command		Yes
Small data move		Yes
CHANGE ROW ADDRESS		Yes
CHANGE READ COLUMN ENHANCED		Yes
READ UNIQE ID	Yes	Yes
COPYBACK	Yes	Yes
READ STATUS ENHANCED	Yes	Yes
GET FEATURES & SET FEATURES	Yes	Yes
Read cache commands	Yes	Yes
PROGRAM PAGE CACHE	Yes	Yes
Number of data bytes per page	2048	8192
Number of spare bytes per page	64	448
Number of bytes per partial page	512	
Numpber of spare bytes per partial page	16	
Number of pages per block	64	128
Number of blocks per LUN	4096	4096
Number of LUNs per chip enable	2	2
Number of address cycles		
Column address cycles	2	2
Row address cycles	3	3
Number of bits per cell	1	1
Bad blocks maximum per LUN	80	80
Block endurance	100000	60,000
Guaranteed valid blocks at beginning	1	1
Block endurance for guranteed valid blocks	0	0
Number of programs per page	4	4
Number of bits ECC correctability	4	8
Number of interleaved address bits	1	1
Interleaved read cache		Yes
Interleaved address restrictions for cache operations	Yes	Yes
Interleaved program cache support	Yes	Yes
Interleaved block address restrictions	No	No
Overlapped/concurrent interleaving	No	No
I/O pin maximum capacitance per target	20 pf/ 10pf	
Driver Strength; Overdrive 1 & 2		Yes
tPROG Typical (Page Program)	600 us	515 us
tBERS Typical (Block Erase)	3 ms	7 ms
tR max (Page Read)	25 us	35 us
tCCS Typical (change column setup)	100 ns	200 ns
Input pin capacitance, typical	10 pf	6 pF

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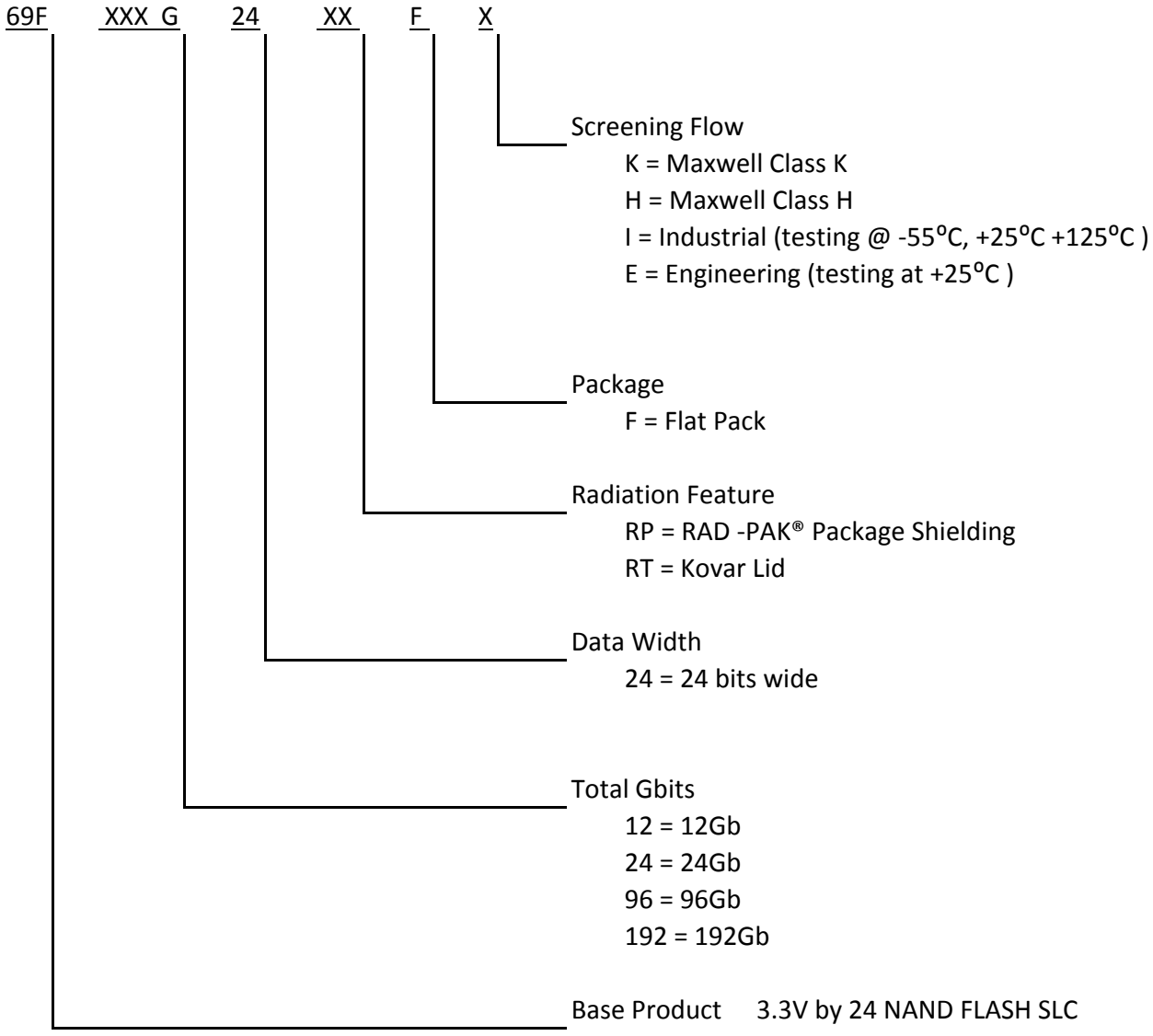
Product Ordering Options



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