

Logic Diagram

FEATURES:

- 14-bit resolution and accuracy
- Total dose hardness:
 - > 100 krad (Si), depending upon space mission
- Single event effects:
 - SEL > 104 MeV/mg/cm²
 - SEU_{TH} = 1.4 MeV/mg/cm²
 - SEU_{Sat} = 1E-3 cm²/Device
- Package:
 - 16 pin RAD-PAK[®] flat package
 - 16 pin RAD-PAK[®] dual-in-line package
- Fast Conversion Times: 10 μs
- Low 50 mW typical power consumption
- High speed LC²MOS technology
 - Analog input range of ±3V
 - 83 KSPS throughput rate
 - Operates with +5V/-5V power supplies
 - 80 dB SNR at 10 kHz input frequency
 - Serial output

DESCRIPTION:

Maxwell Technologies' 7872 high-speed 14-bit ADC microcircuit features a greater than 100 krad (Si) total dose tolerance; depending upon orbit. The 7872 consists of a track/hold amplifier, successive-approximation ADC, 3V buried Zener reference and versatile interface logic. It features a self-contained, laser-trimmed internal clock, so no external clock timing components are required. To achieve the minimum noise possible, the on-chip clock may be overridden to synchronize the device operation to the digital system. The 7872 is a serial output device. It is capable of interfacing to all modern microprocessors and digital signal processors. The 7872 operates from ±5V power supplies, accepts bipolar input signals of ±3V and is able to convert full power signals up to 41.5 kHz. It is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Maxwell Technologies' patented RAD-PAK[®] packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK[®] provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies' self-defined Class S.

TABLE 1. 7872 PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	CONTROL	Control Function
2	$\overline{\text{CONVST}}$	Convert Start
3	CLK	Clock Input
4	$\overline{\text{SSTRB}}$	Serial Strobe
5	SCLK	Serial Clock
6	SDATA	Serial Data
7	NC	Non Connect
8	DGND	Digital Ground
9	V _{DD}	Positive Supply
10	NC	No Connect
11	C _{REF}	Reference Capacitor
12	AGND	Analog Ground
13	REF _{OUT}	Voltage Reference Output
14	V _{IN}	Analog Input
15	V _{SS}	Negative Supply
16	V _{DD}	Positive Supply

TABLE 2. 7872 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Positive Supply Voltage; Relative to GND	V _{DD}	-0.3	7.0	V
Negative Supply Voltage; Relative to GND	V _{SS}	+0.3	-7.0	V
AGND to DGND; Relative to GND	--	-0.3	V _{DD} +0.3	V
REF _{OUT} , C _{REF} to AGND	--	0	V _{DD}	V
V _{IN} to AGND	--	V _{SS} -0.3	V _{DD} +0.3	V
Digital Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Digital Output Voltage	V _{OUT}	-0.3	V _{DD} +0.3	V
Weight		--	2.0	Grams
Thermal Impedance	Θ_{JC}	--	2.44	°C/W
Storage Temperature Range	T _S	-65	150	°C
Operating Temperature Range	T _A	-55	125	°C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{DD}	$\pm 10\%$
I_{SS}	$\pm 10\%$

1. Parameters are measured and recorded as Deltas per MIL-STD-883 for Class S Devices, specified in Table 10.

TABLE 4. 7872 DC ELECTRICAL CHARACTERISTICS FOR DYNAMIC PERFORMANCE ¹

($V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, $AGND = DGND = 0\text{ V}$, $f_{CLK} = 2\text{ MHz EXTERNAL}$, $f_{SAMPLE} = 83\text{ kHz}$, $-55\text{ TO }125\text{ }^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Signal to Noise Ratio $V_{IN} = 10\text{kHz}$ Sine Wave, T_{MIN} to T_{MAX} ; SNR is typically 82dB for $V_{IN} < 41.5\text{kHz}$ ²	SNR	4, 5, 6	79	--	--	dB
Total Harmonic Distortion $V_{IN} = 10\text{kHz}$ Sine Wave	THD	4, 5, 6	--	-86	--	dB
Peak Harmonic or Spurious Noise	--	4, 5, 6	--	-86	--	dB
Intermodulation Distortion Second Order Terms: $f_a = 9\text{ kHz}$, $f_b = 9.5\text{ kHz}$, $f_{SAMPLE} = 50\text{ kHz}$ Third Order Terms: $f_a = 9\text{ kHz}$, $f_b = 9.5\text{ kHz}$, $f_{SAMPLE} = 50\text{ kHz}$	IMD	4, 5, 6	--	-86	--	dB
Track/Hold Acquisition Time	--	9, 10, 11	--	--	2	μs

- $V_{IN} = \pm 3\text{ V}$. Guaranteed by design.
- SNR calculation includes distortion and noise components.

TABLE 5. 7872 DC ELECTRICAL CHARACTERISTICS FOR ACCURACY

($V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, $T_A = -55\text{ TO }125\text{ }^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Resolution	RES	7, 8A, 8B	14	--	--	Bits
Resolution for Which No Missing Codes are Guaranteed	NMC	7, 8A, 8B	14	--	--	Bits
Integral Nonlinearity @ $25\text{ }^\circ\text{C}$	INL	1, 2, 3	--	± 1	--	LSB
Integral Nonlinearity T_{MIN} to T_{MAX}	INL	1, 2, 3	--	--	± 2	LSB
Bipolar Zero Error	BZE	1, 2, 3	--	--	± 12	LSB
Positive Gain Error ¹	PGE	1, 2, 3	--	--	± 12	LSB
Negative Gain Error ¹	NGE	1, 2, 3	--	--	± 12	LSB

- Measured with respect to internal reference.

TABLE 6. 7872 DC ELECTRICAL CHARACTERISTICS FOR ANALOG INPUT

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125 \text{ } ^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Input Voltage Range	--	1, 2, 3	-3	3	V
Input Current	--	1, 2, 3	-500	500	μA

TABLE 7. 7872 DC ELECTRICAL CHARACTERISTICS FOR REFERENCE OUTPUT

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125 \text{ } ^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
REF _{OUT} @ +25 °C	--	1	2.99	3.01	V
REF _{OUT} T _{MIN} to T _{MAX}	--	2, 3	2.98	3.02	V
REF _{OUT} Tempco: Typically 35ppm ¹	--	1, 2, 3	--	± 40	ppm/ $^\circ\text{C}$
Reference Load Sensitivity (DREF _{OUT} /DI) Reference Load Current Change (0-300 μA); Reference Load Should Not Be Changed During Conversion	--	1, 2, 3	--	1.2	mV

1) Characterized, Not 100% Tested

TABLE 8. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC INPUTS

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125 \text{ } ^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Input High Voltage: $V_{DD} 5V \pm 5\%$ ²	V _{INH}	1, 2, 3	2.4	--	V
Input Low Voltage: $V_{DD} 5V \pm 5\%$ ²	V _{INL}	1, 2, 3	--	0.8	V
Input Current: (CONVST) V _{IN} = 0 V to V _{DD}	I _{IN}	1, 2, 3	-10	10	μA
Input Current: (Control, Clk) V _{IN} = V _{SS} to V _{DD}	I _{IN}	1, 2, 3	-10	10	μA
Input Capacitance ¹	C _{IN}	1, 2, 3	--	10	pF

1) Not Tested

2) Application of Signal

TABLE 9. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC OUTPUTS

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125 \text{ } ^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Output Low Voltage I _{SINK} = 1.6 mA	V _{OL}	1, 2, 3	--	0.4	V

TABLE 10. 7872 DC ELECTRICAL CHARACTERISTICS FOR CONVERSION TIME

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125 \text{ } ^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
External Clock ¹	--	9, 10, 11	--	10	μs
Internal Clock: Nominal Value = 2 MHz	--	9, 10, 11	--	11	μs

1) Application of Signal

TABLE 11. 7872 DC ELECTRICAL CHARACTERISTICS FOR POWER REQUIREMENTS

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 to 125 °C UNLESS OTHERWISE SPECIFIED)

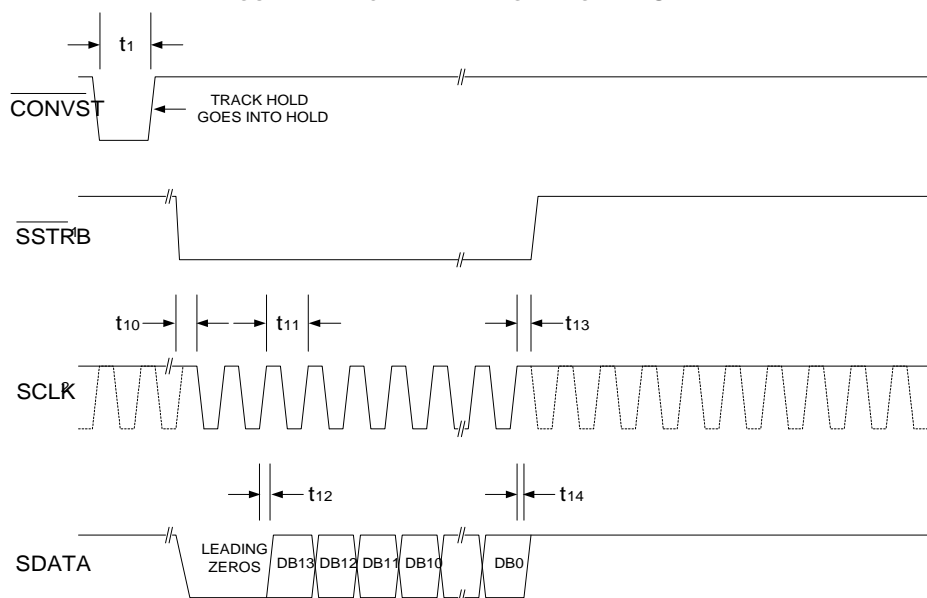
PARAMETER	SYMBOL	CONDITIONS	SUBGROUPS	REQUIREMENTS	UNITS
Positive Supply Voltage	V _{DD}	5% for Specified Performance	--	5	V
Negative Supply Voltage	V _{SS}	5% for Specified Performance	--	-5	V
Positive Supply Current	I _{DD}	Typically 6mA	1, 2, 3	13	mA max
Negative Supply Current	I _{SS}	Typically 4mA	1, 2, 3	6	mA max
Power Dissipation	P _D	Typically 50mW	1, 2, 3	95	mW max

TABLE 12. 7872 TIMING CHARACTERISTICS ^{1,2}(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 to 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER/CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
CONVST Pulse Width	t ₁	9, 10, 11	50	--	ns
SSTRB to SCLK Falling Edge Setup Time	t ₁₀	9, 10, 11	100	--	ns
SCLK Cycle Time ³	t ₁₁	9, 10, 11	440	--	ns
SCLK to Valid Data Delay: C _L = 35 pF ⁴	t ₁₂	9, 10, 11	--	155	ns
SCLD Rising Edge to SSTRB	t ₁₃	9, 10, 11	20	150	ns
Bus Relinquish Time After SCLK	t ₁₄	9, 10, 11	4	100	ns

1. All input signals are specified with tr = tr = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
2. Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and SSTRB and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
3. SCLK mark/space ration (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
4. SDATA will drive higher capacitive loads, but this will add to t₁₂ since it increases the external RC time constant (4.7kΩ/C_L) and hence, the time to reach 2.4 V.

FIGURE 1. MODE 1 TIMING DIAGRAM SERIAL



1. External 4.7 k Ω pull-up resistor.
2. External 2 k Ω pull-up resistor continuous SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V.

FIGURE 2. LOAD CIRCUIT FOR ACCESS TIME

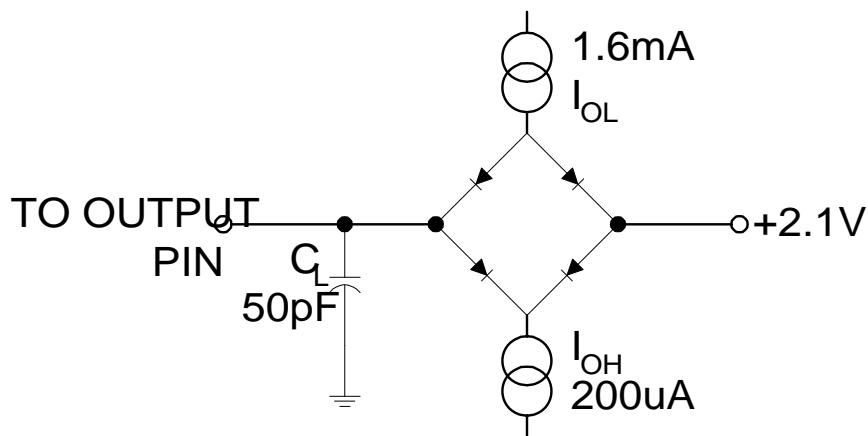
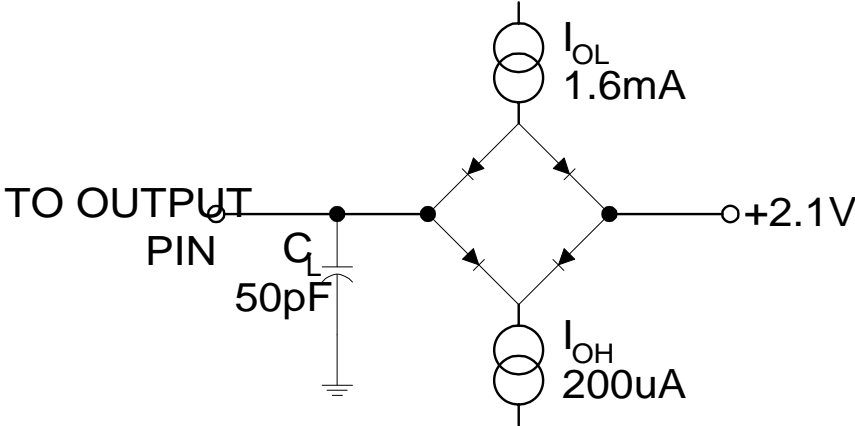
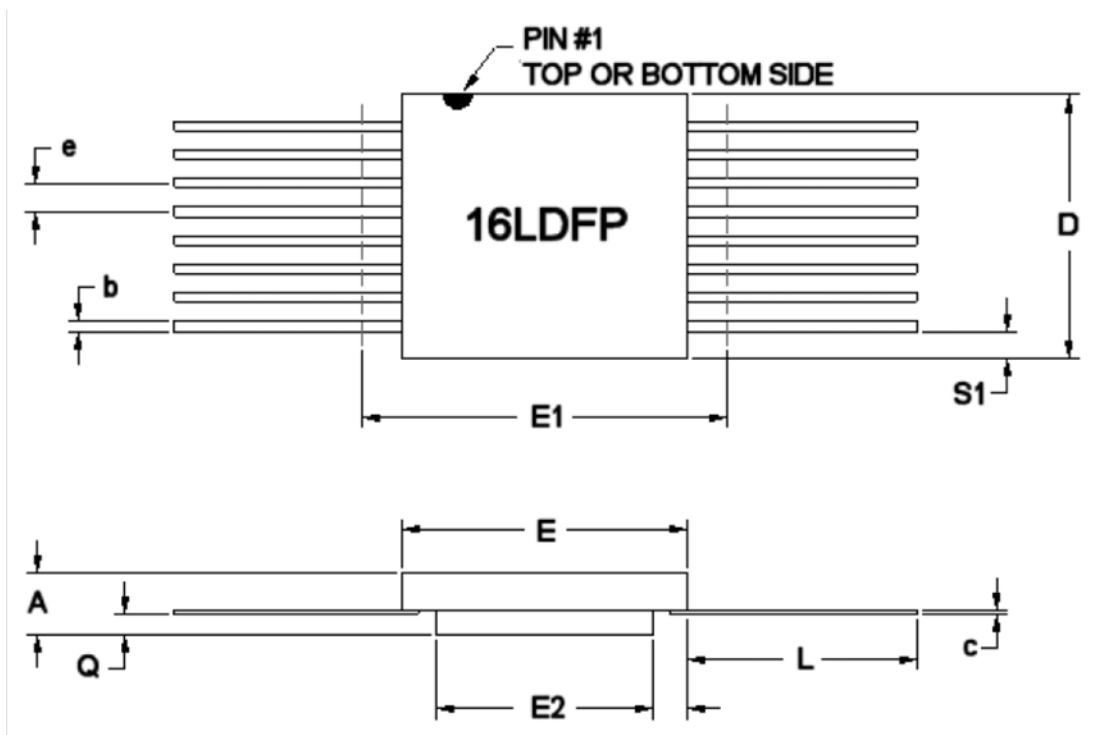


FIGURE 3. LOAD CIRCUIT FOR OUTPUT FLOAT DELAY

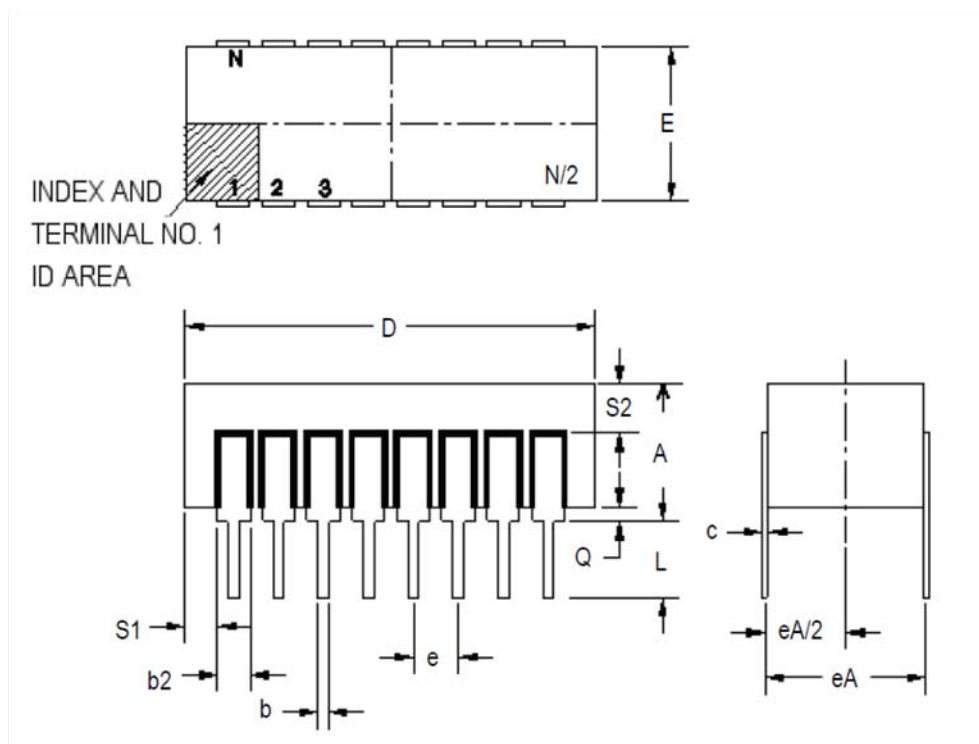




16 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.115	0.135	0.150
b	0.015	0.017	0.019
c	0.004	0.005	0.007
D	0.407	0.415	0.423
E	0.275	0.280	0.285
E1	--	--	0.500
E2	0.150	0.156	0.162
E3	0.030	0.062	--
e	0.050 BSC		
L	0.325	0.335	0.345
Q	0.020	0.033	0.045
S1	0.005	0.024	0.045
N	16		

Note: All dimensions in inches
The top and bottom of the package connected to -V.



16 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.157	0.200
b	0.014	0.018	0.026
b2	0.045	0.047	0.065
c	0.008	0.010	0.018
D	--	0.800	0.840
E	0.220	0.295	0.310
eA	0.300 BSC		
eA/2	0.150 BSC		
e	0.100 BSC		
L	0.135	0.145	0.155
Q	0.000	0.002	0.060
S1	0.005	0.027	--
S2	0.005	--	--
N	16		

Note: All dimensions in inches
The top and bottom of the package connected to -V.

Important Notice:

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