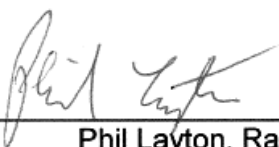



SEE Radiation Test Report

Part Type:	48SD1616, 97SD3232, 97SD3240, 97SD3248
Manufacturer:	Maxwell Technologies
Die Part No.:	HM5225405B
Die Manufacturer:	Elpida
Document No.:	1003857
Revision:	1
Date:	April 21, 2003

Prepared by:  Date: 4/21/03
Phil Layton, Radiation Scientist

Reviewed by:  Date: 4/21/03
Gale Williamson, Electrical Engineering Manager

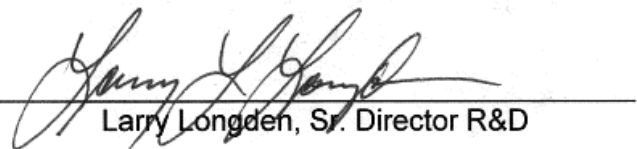
Reviewed by:  Date: 4/22/03
Larry Longden, Sr. Director R&D

Table of Contents

Purpose

Abstract

Introduction

Test Methodology

Data

Comparison

Summary

Conclusion

Appendix

PURPOSE

This report presents a summary of radiation data on the Elpida/Hitachi HM5225405B (16M x 4Banks x 4Bits), 256 Megabit SDRAM die used in Maxwell's SDRAM product line; the 48SD1616, 256 Megabit SDRAM, and the 97SD3232/3240/3248 multichip module family representing 1.0/1.28/1.5 Gigabits respectively. Single event effects (SEE) data including SEL, SEFI & SEU are summarized below.

ABSTRACT

The Elpida 256 Megabit SDRAM has been tested for SEE and found to be suitable for space applications using a double device error detection and correction technique. The occurrence of SEFI's drives the requirement for error detection and correction from the bit level, typical for other memories, to the device level. The presence of control logic in SDRAM leads to upsets that can temporarily disrupt device functionality. This, combined with the probability of a single bit upset (SBU) or multiple bit upset (MBU) in another device, drives the need for double device correction.

The SEL threshold is greater than 85 MeV-cm²/mg at room temperature (25 °C) and decreases to 55 MeV-cm²/mg at 85 °C. This corresponds to a SEL rate in a geosynchronous orbit (worst case environment for heavy ions) of one latchup in 20,000 years operating at 85 °C, which is the worst case SEL temperature. The SEFI saturated cross-section is approximately 4 E-4 cm²/device with a threshold around 20 MeV-cm²/mg. The SEFI rate in a geosynchronous orbit (worst case environment for heavy ions) is once every 8 years. Parts programmed in the inverse bleed down pattern have the highest probability of SEU's. The inverse bleed down SEU saturated cross-section is 2 E-9 cm²/bit, with a SEU threshold of approximately 2.7 MeV-cm²/mg. The proton cross-section at 92.5 MeV is approximately 3 E18 cm²/bit. This die is not subject to MBU's, SEL's or SEFI's from protons. Utilizing a Reed-Solomon error detection and correction scheme, the single event error rate due to all effects drops from 5 times a year to once every 6 million years.

INTRODUCTION

SDRAM technology represents the state of the art in high-density, volatile memory. SDRAM's have a complex internal architecture that both controls their operation and affects their susceptibility to radiation effects. Internal control logic causes MBU's and SEFI's, not common to previous generation memory devices. Consequently, these conditions should be fully characterized before an effective mitigation strategy can be chosen. Figure 1 shows a block diagram of a 256 Megabit SDRAM's internal architecture.

SDRAM operations are row based. Rows are activated before reads and writes can occur, then deactivated or "precharged" after completion of a read or write cycle in that row. To maintain the integrity of the data, the memory needs to be "refreshed", or in other words, charge needs to be added. As the operating temperature increases, the rate at which each row needs to be refreshed also increases. To conserve power, the device can be set into multiple power-saving modes. The internal state machine controls synchronous burst reads

and writes, while the mode register is used to set operational parameters such as CAS latency and word burst length.

Block Diagram

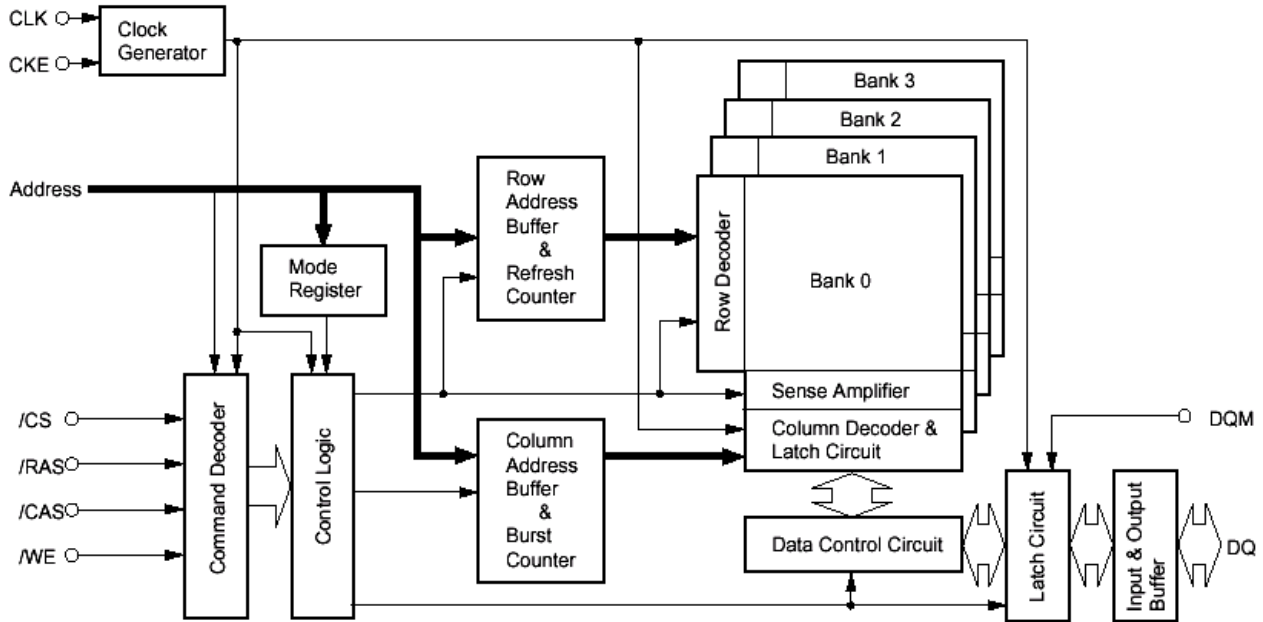


Figure 1. Block diagram of 256 Megabit SDRAM Internal Architecture

Because an error could occur in any, or all of these various states, the vulnerable modes and parameters of these modes need to be well understood.

To read or write to a memory row, the following process should be followed: the device starts in an idle state, the row is then activated, next the row is read or written to, the row is then precharged when complete, finally returning the SDRAM to an idle state. To maintain charge on the memory, there are two basic refresh modes: Auto Refresh and Self Refresh. Auto Refresh lets software or firmware control the refresh rate, as compared to Self Refresh, in which the device refreshes itself continuously using an internal clock. To maintain the memory integrity, the refresh rate has to be increased with increasing temperature. We discovered that above 72 °C, the self-refresh mode is too slow to retain the memory contents in the cells and consequently, the refresh rate has to increase to compensate. Moreover, there is a “bleed down pattern” towards which the data will relax to a known state if the part is not refreshed. As will be discussed later, the “bleed down pattern” directly affects the SEU rate.

TEST METHODOLOGY

TEST GOALS

The goals of the single event effects tests were: 1) to evaluate a selection of the latest commercial SDRAM die to determine which has the best single event, and specifically, SEL characteristics, 2) to fully characterize the selected SDRAM die for SEL, SEU & SEFI radiation response, and 3) to identify any other anomalies such as temperature and refresh rate dependencies. A detailed test plan consisting of multiple single event tests was developed to evaluate the performance of the SDRAM die. Pre-radiation testing was performed to evaluate refresh rate as a function of temperature. During testing, we looked at: single versus multiple bit upsets, sensitivity of memory cells to the bleed down pattern (i.e. any preference of bit flip errors from a "1" to a "0" or a "0" to a "1") and dependency of errors to either temperature and/or refresh rate. In addition to the above, SEFI's were evaluated for both quantity and type of errors, as to whether the entire word was upset and whether the errors were recoverable with or without a power cycle, or from different idle modes. In addition, we looked at recoverable and non-recoverable high-current states relating to SEFI's. To evaluate mitigation techniques, we analyzed the effects of mode register resets and initializations. Finally, SEL was measured as a function of temperature and ion fluence.

TEST APPROACH

We used a JDI tester to power a specially designed daughter board to drive the parts, as well as to test for SEU's and SEFI's. The tests described below were characterized over LET's ranging from 2.7 to 85 MeV-cm²/mg. SEL was tested by measuring the supply current and then triggering off of a preset current value. A heater and temperature sensor were placed on each DUT board to test for potential temperature-dependent effects. Figure 2 shows the SDRAM test board being irradiated in an open-air environment at Texas A&M's Cyclotron facility.



Figure 2. SDRAM test board irradiated at Texas A&M's Cyclotron

A software program was developed to fully exercise the parts in both static and dynamic modes.

The static mode tests the part with idle loops and periodic auto refreshes. The test sequence used for the static mode was:

- 1) Initialize and verify device with bleed down or inverse bleed down pattern
- 2) Start cycle of idle with auto refreshes
- 3) Turn on beam
- 4) Turn off beam
- 5) Count memory errors

In the dynamic test, the memory cells were written using two words per row (burst length of 2) with a write to the entire memory then read and compare, with column fast addressing to

unmask errors associated with row based SDRAM operations. The test sequence used for the dynamic mode was:

- 1) Initialize and verify part
- 2) Start dynamic test sequence
- 3) Turn on beam
- 4) Turn off beam
- 5) Count memory errors

The following modes were tested in dynamic mode: Auto refresh Idle, Auto Refresh Power Down, Write then Read to the Inverse Bleed Down Pattern, and Write then Read to the Bleed Down Pattern.

Maxwell built a resistive heating element with a thermal controller placed underneath the package to test for temperature dependency of SEL, SEU's and SEFI's. The temperature was measured with a thermocouple and controlled through an external temperature control unit.

Because of the size of the memory and the time required to read and write to all the cells, only some of the errors were recorded and stored, whereas all the errors were counted. The recorded errors allowed for analysis of the number of errors per word and the location of the errors, as well as other statistics such as the probability of a bit flipping from a 1 to 0 or a 0 to 1. Some of the testing was conducted on all four banks to correlate results with the majority of the testing, which was conducted on only one bank at a time.

PART PROCESSING

For the initial radiation testing, bare die was not readily available in small quantities from most manufacturers and as a result, a combination of plastic parts and bare die were used. All of the plastic devices tested had wire bond pads down the middle of the die connected to a metal lead frame. This lead frame has the potential to create a shielding issue for heavy ions and therefore, could potentially affect the SEE test results. As a result, we believed it was essential to remove the lead frame prior to heavy ion testing.

To expose the die of the SDRAM plastic parts, the initial processing required etching away the entire plastic package and then removing the lead frame, while maintaining the integrity of the bond pads. The depotted die was subsequently rebonded to a specially designed test board, allowing full exposure to the die surface. Figure 3 shows one of the original plastic parts that was depotted with the lead frame removed and then re-wire bonded. These "depotted die" were used for both the initial test at Brookhaven National Laboratory, as well as the first test at Texas A&M.

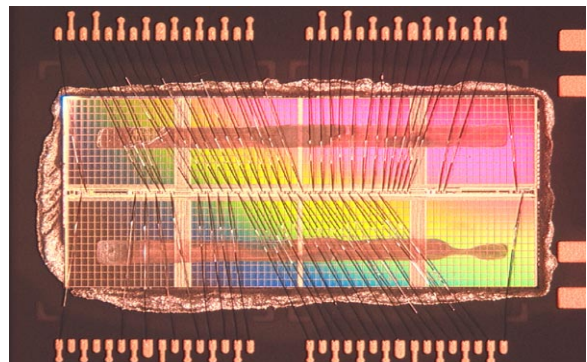


Figure 3. Depotted plastic SDRAM used at first Brookhaven National Laboratory Test

Depotting proved to be a very difficult process because the etching chemical (fuming Nitric acid) had a tendency to degrade the bond pads. Additionally, any residual acid left on the die created potential reliability issues over time since the die would be subject to a continual slow etching. For the 3 subsequent tests at Texas A&M, Maxwell was able to acquire a wafer of Elpida die, the die was wire bonded and packaged at Maxwell Technologies to be used for subsequent radiation characterization.

PART SELECTION

Maxwell uses SEL as the first gate that must be passed through for a part to be considered usable in space. Because latchup requires power cycling and has the greatest potential—with respect to single event effects—to be catastrophic, we set certain SEL thresholds that a device must meet in order for it to be considered for additional radiation testing. Table 1 shows a summary of the four manufacturers we evaluated for SEL threshold. If a device meets or exceeds this threshold, the next radiation tests we perform on a device are for other single event effects, such as SEFI's and SEU's. Usually, upsets can be mitigated through the inclusion of an error detection and correction method. Finally, we irradiate the parts for total ionizing dose, to better understand how they will function in a representative space mission environment.

Manufacturer	SEL Threshold (MeV-cm ² /mg)
Elpida	>82
B	<60
C	<60
D	<36

Table 1. SEL threshold evaluation summary at 25 °C

Because Maxwell's RAD-PAK® packaging technology has the ability to improve upon a die's inherent tolerance to TID, we are able to select the manufacturer based upon the best SEE results. In this particular case, after the initial SEE screening, this method allowed us to obtain "evaluation" wafers from Elpida, which we then diced and wire bonded onto a printed circuit board. By procuring die, we are able to characterize die lot specific effects. Figure 4 and Figure 5 show the 256 SDRAM die used in some of the SEE tests and which will be offered in Maxwell's SDRAM products.



Figure 4. Top view of die layout



Figure 5. Die part marking

DATA

SINGLE EVENT EFFECTS

Maxwell performed four separate heavy ion SEE tests. The first test was conducted at Brookhaven National Laboratories Van de Graff generator using depotted plastic parts and bare die that were subsequently wire-bonded to a PCB test board. The other three tests were conducted at Texas A&M's Cyclotron facility, with the first test using depotted plastic parts, as opposed to the second and third tests which used bare die from an evaluation wafer that were wire-bonded to pcb test boards.

SEL

At room temperature, there were no latchups seen in any of the tests. The highest LET level attained at Brookhaven was 82 MeV-cm²/mg and the highest LET level attained at TAMU was 85 MeV-cm²/mg. Recoverable high current states were seen at an LET level of 69 MeV-cm²/mg at 100° C during the first test at TAMU using depotted die. At first, the high current event appeared to be a latchup. However, when the flux was reduced to around 1E3 particle/cm²-sec, it was discovered that the device was recovering within one write/read cycle which had contained a mode register reset. Therefore, these were identified as SEFI related

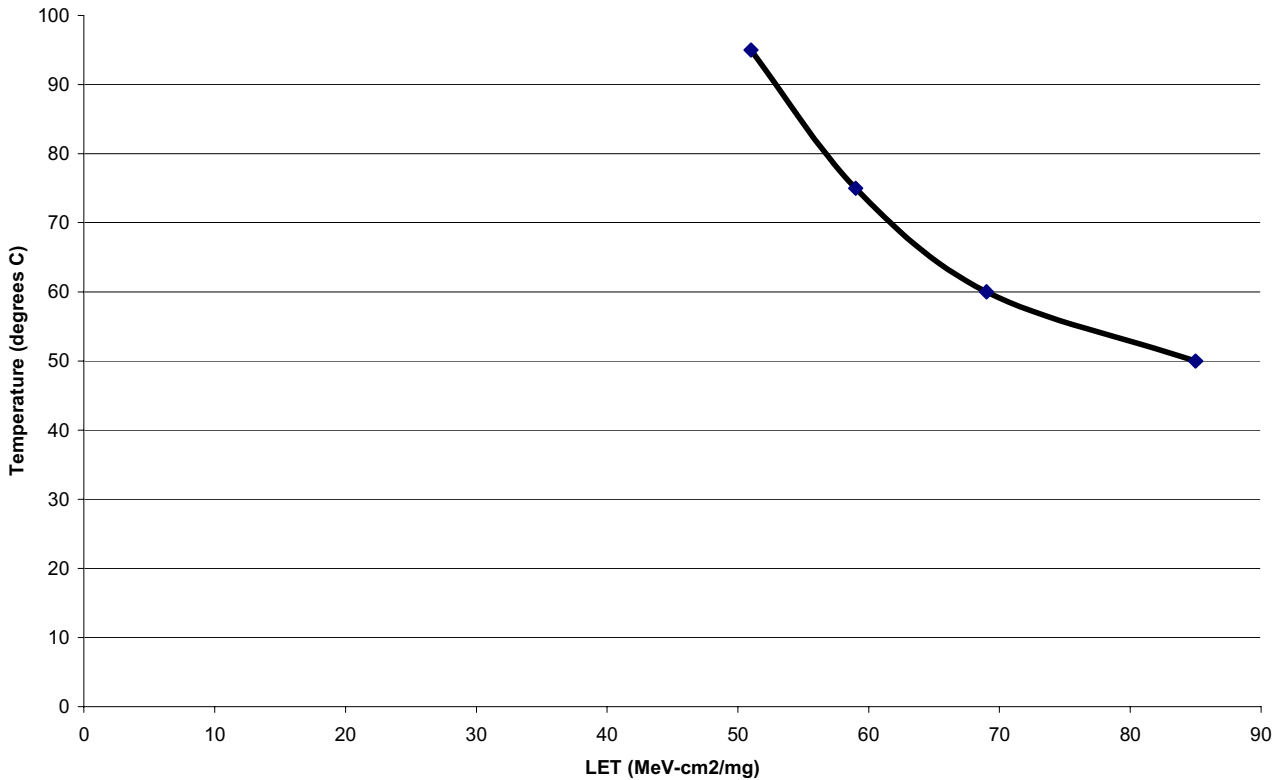


Figure 6. SEL versus temperature

and will be discussed in the following section. In a subsequent test using bare die, latchups occurred that required a power cycle. These latchups were characterized as a function of

LET and temperature and are graphed in Figure 6. In the temperature evaluation test, two parts were tested, each to a fluence of $1 \text{ E6 particles/cm}^2$. The graph represents the first latchup seen at each of the temperatures and LET levels. In all cases, only one of the two parts actually latched at these levels, with the other part latching at a slightly higher temperature. Cross-sections ranged from 1 E-6 to $3 \text{ E-6 cm}^2/\text{device}$.

SEFI

One of the difficulties encountered in our test and one that has also been described in published reports, is the ability to distinguish between a SEU and a SEFI. Initial classification of the errors was determined by measuring the current and number of errors in memory. Subsequent analysis included location of the errors and response of the errors to MRS and temperature variations. SEFI's were indicative of a large number of errors in sequential rows, typically several rows that were next to each other would have a similar number of errors. Tests were run where the memory was continually written to and read. The number of errors was derived by a comparison of what was expected in a particular location and the actual contents that were read from the memory. During a run, a sudden jump in the number of recorded errors would indicate a SEFI.

Two types of SEFI's were observed. The first type of SEFI, that we named "Logic SEFI", generated less than 5000 errors per bank and is considered to be a row-based error. Logic SEFI's corrupted the memory and sometimes required a MRS to recover, while other times required only a write read cycle to recover. The second SEFI type, referred to as a "State Machine SEFI", was characterized of having greater than 50,000 errors, appeared to occur over entire columns, and required a MRS to recover.

State Machine SEFI's usually appeared on the tester as a complete memory failure. However, after a MRS the tester showed around 200,000 to 500,000 errors which suggested a loss of data from a combination of corrupted bits and missed refresh cycles when the memory was non-operational. Therefore, it appears that although the State Machine SEFI's corrupt control logic, they may not necessarily corrupt memory locations—as long as the refresh rate is maintained. In addition, since the refresh rate can't be maintained during this type of SEFI, there may not be an effective way to recover those corrupted memory locations. Finally, the State Machine SEFI's occurred at higher LET's, and less often, in comparison to the other SEFI's.

There were several types of Logic SEFI's; one type was accompanied by an increase in standby current of approximately 0.5 mA to 2 mA. This type of Logic SEFI is temperature sensitive. When the beam was turned off and the part was operating at a higher temperature of 85 °C, the high current state would return once the beam was turned on again and required a MRS to return to normal operating current. However, when the temperature was lowered to 30 °C, the current would recover after the beam was turned off and but didn't require a MRS. Another type of Logic SEFI did not have an increased current state, but would require a MRS to recover.

Figure 7 shows the Logic SEFI rate as a function of LET. Data was also taken over various temperatures and showed an actual downward trend for Logic SEFI rates that correlates with increasing temperature. The saturated Logic SEFI cross-section is approximately 4 E-4

cm²/device. The State Machine SEFI's occurred at higher LET's, starting at around 40 MeV-cm²/mg and with a saturated cross-section around 2 E-5 cm²/device, which is a cross-section roughly an order of magnitude less than that of Logic SEFI's. Therefore, the overall SEFI rate is dominated by the Logic SEFI rate.

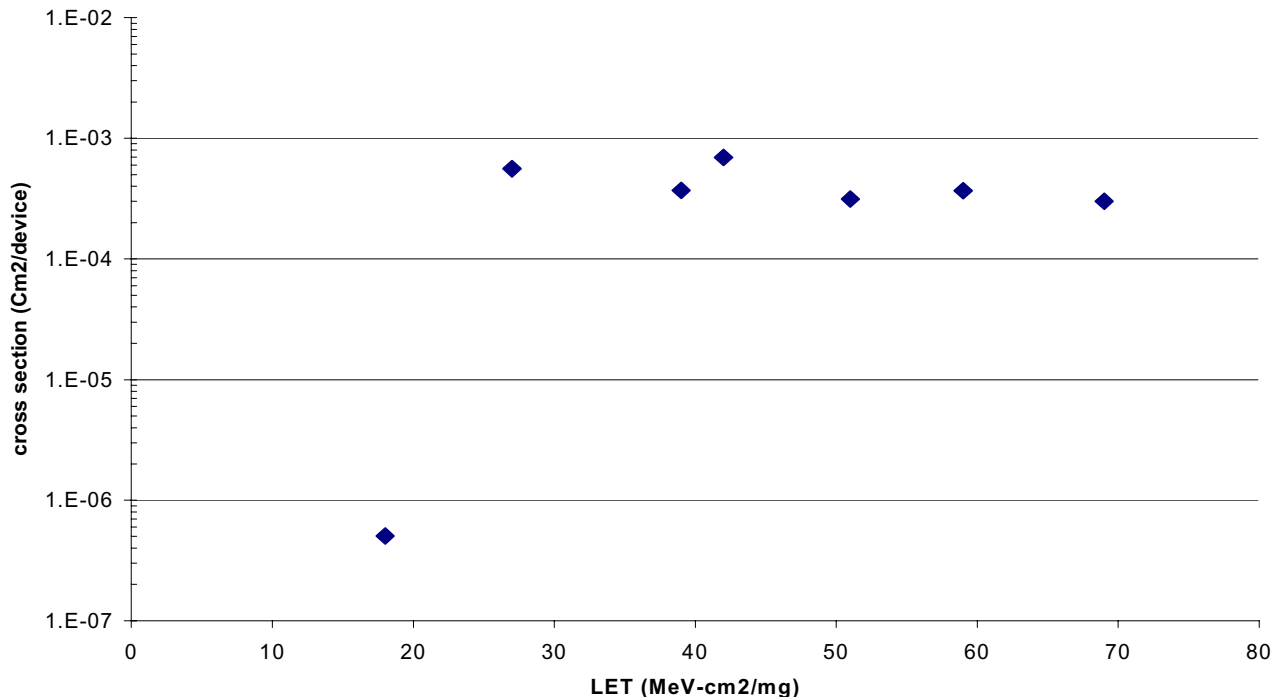


Figure 7. Heavy ion Logic SEFI cross-section

A test was conducted to verify if a SEFI would improperly drive data lines when sharing the data bus width another connected SDRAM device. A control DUT that was electrically connected to the irradiated part confirmed there were no errors propagating to the other device, even after multiple SEFI's were generated on the irradiated part at an LET of 69 MeV-cm²/mg and a fluence of 4.6 E 6 particles/ cm².

SEU

Testing revealed that the SEU rate depended on whether the part was programmed with the bleed down pattern or inverse bleed down pattern. We conducted extensive testing to determine the bleed down pattern of the SDRAM die. This was accomplished by leaving the memory in an unrefreshed mode and then reading the memory. Table 2 shows the natural pattern that the memory cells return to when not refreshed (recharged). The tendency is for the entire row to bleed down to all "0's" or all "F's".

SEU's were distinguished from SEFI's by looking at the number of errors per word. More than two errors in a word that were also accompanied by multiple rows, where the majority of the word had an error, were considered to be caused by a SEFI. All other errors were considered to be SEU's.

Row	Column				
	0	1	2	3
7	FFFF	FFFF	FFFF	FFFF	FFFF
6	FFFF	FFFF	FFFF	FFFF	FFFF
5	0000	0000	0000	0000	0000
4	0000	0000	0000	0000	0000
3	FFFF	FFFF	FFFF	FFFF	FFFF
2	FFFF	FFFF	FFFF	FFFF	FFFF
1	0000	0000	0000	0000	0000
0	0000	0000	0000	0000	0000

Table 2. Natural “bleed down” pattern for SDRAM

Figure 8 shows the cumulative error rates over three separate runs at Texas A&M and the SEU cross-section compilation from all the tests comparing the inverse bleed down pattern to the bleed down pattern. As can be seen by the graph, the bleed down pattern has a cross-section over an order of magnitude lower than the inverse bleed down pattern. Additionally, for the inverse bleed down pattern there is a preference for errors going from 1’s to 0’s. An analysis from Maxwell’s second TAMU test shows a range of 70% to 76% preference of errors going from 1’s to 0’s. The “inverse bleed down” SEU saturated cross-section is 2 E-9

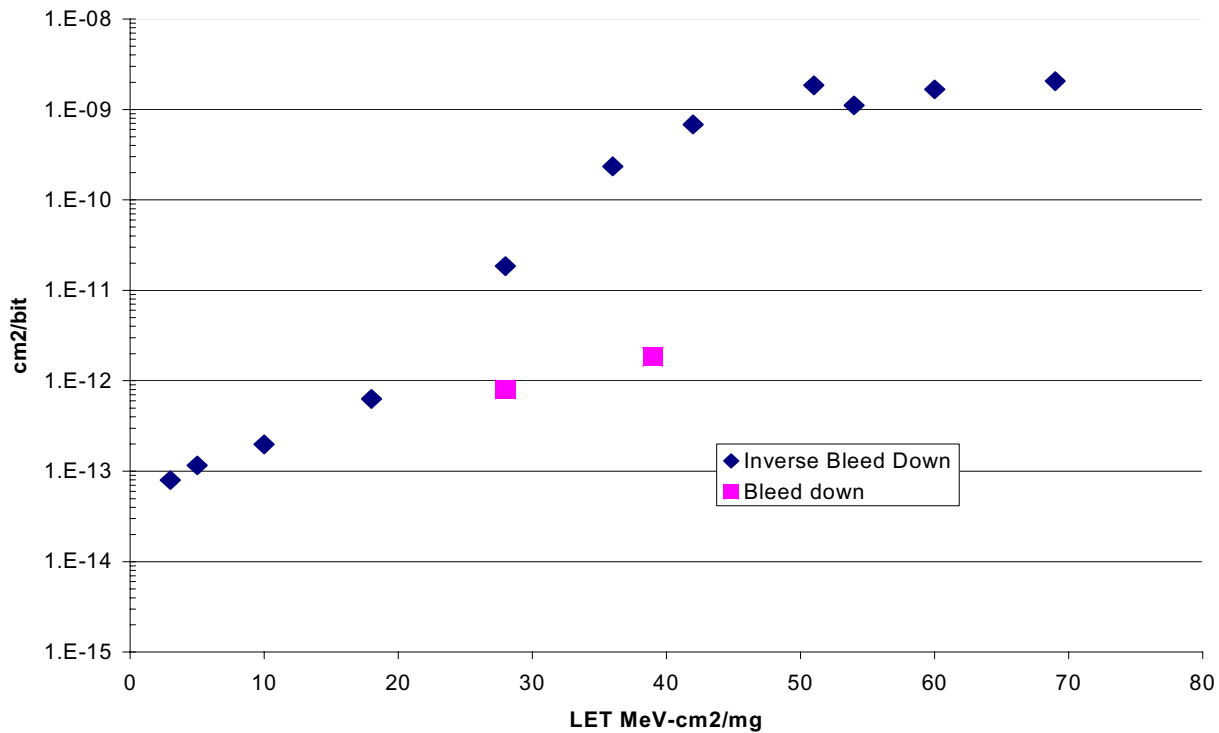


Figure 8. SEU cross-section showing inverse bleed down pattern and bleed down pattern.

cm²/bit. By extending the curve, the “bleed down” saturated cross-section appears to be around 5E-11 cm²/bit, approximately an order of magnitude lower than the “Inverse Bleed

Down” saturated cross-section. The variability in SEU cross-sections was up to an order of magnitude difference for some of the LET values. Testing was complicated by stuck bits and the variability of SEU rates between different parts. Some of the variability was associated with differentiating SEFI’s from SEU’s. If a SEFI occurs, there are a certain number of SEU’s that occurred in the memory which were not counted. Even at LET’s below 20 MeV-cm²/mg where we didn’t see any SEFI’s, there was roughly a 2X variability in the cross section.

STUCK BIT

Stuck bits are cells that temporarily cannot be programmed, they are discussed in more detail in R. Koga’s paper[10]. The number of stuck bits and relaxation time was evaluated after irradiation by heavy ions. Susceptibility to stuck bits was tested in the inverse bleed down and bleed down mode by looking at errors after the beam was turned off and while the memory was continually written to and read. The part had received 3 krad (Si) of total dose by the time the beam was turned off. Figure 9 shows the relaxation of stuck bits after 30 minutes tested at room temperature.

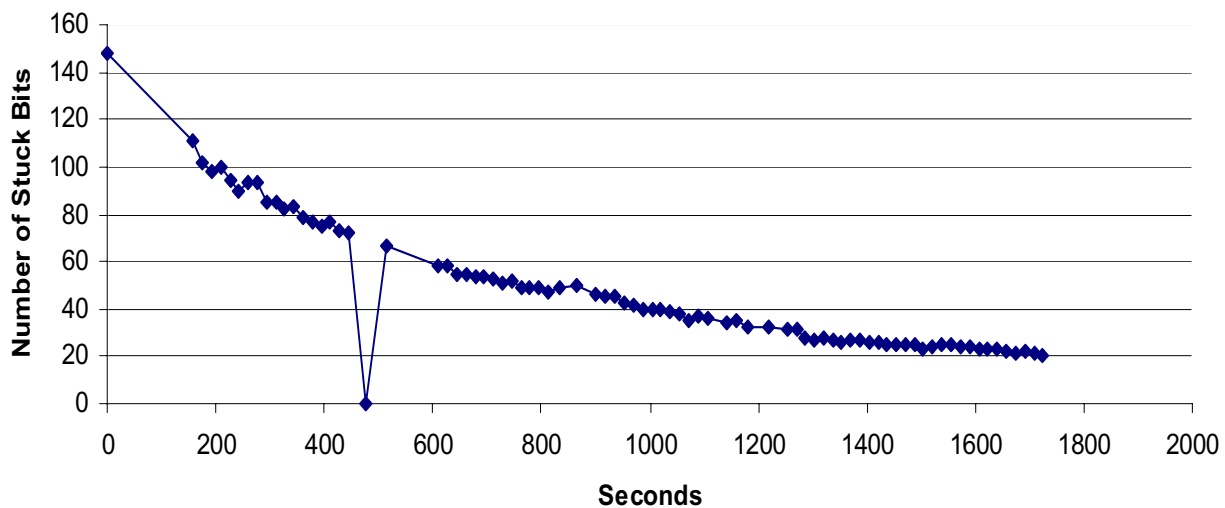


Figure 9. Stuck Bit relaxation time in seconds

The number of bits that were unable to correctly be written to decreases with time, showing an annealing of the free charge. At about 500 seconds, the part was programmed in the bleed down pattern and there were no errors. Then the part was programmed again in the inverse bleed down mode and the number of errors resumed to fit the same relaxation curve shown in Figure 9. Typically, there were less than 50 stuck bits following a test run, however, on two occasions more than 100 stuck bits were observed. Figure 9 shows one of the two occasions when there were over 100 stuck bits. Ninety percent of the stuck bits returned a programmable state in less than an hour. Stuck bits appear to be cells whose ability to hold charge is weakened temporarily or a build up of charge in the oxide. This “stuck bit” phenomenon is directly proportional to temperature and inversely proportional to refresh rate.

PROTON TESTING

Hirex [5] performed proton testing on the same Hitachi (now Elpida) 256 Megabit SDRAM die referenced in this report and used by Maxwell in its SDRAM products. They found no multiple bit upsets with protons and very few single bit upsets in the tested range of 60.2 to 92.5 MeV protons. Fluences ranged between 7 E9 and 2 E10 protons/cm². In addition, there were no upsets at the low energy of 39.2 MeV. The cross-section at 92.5 MeV is

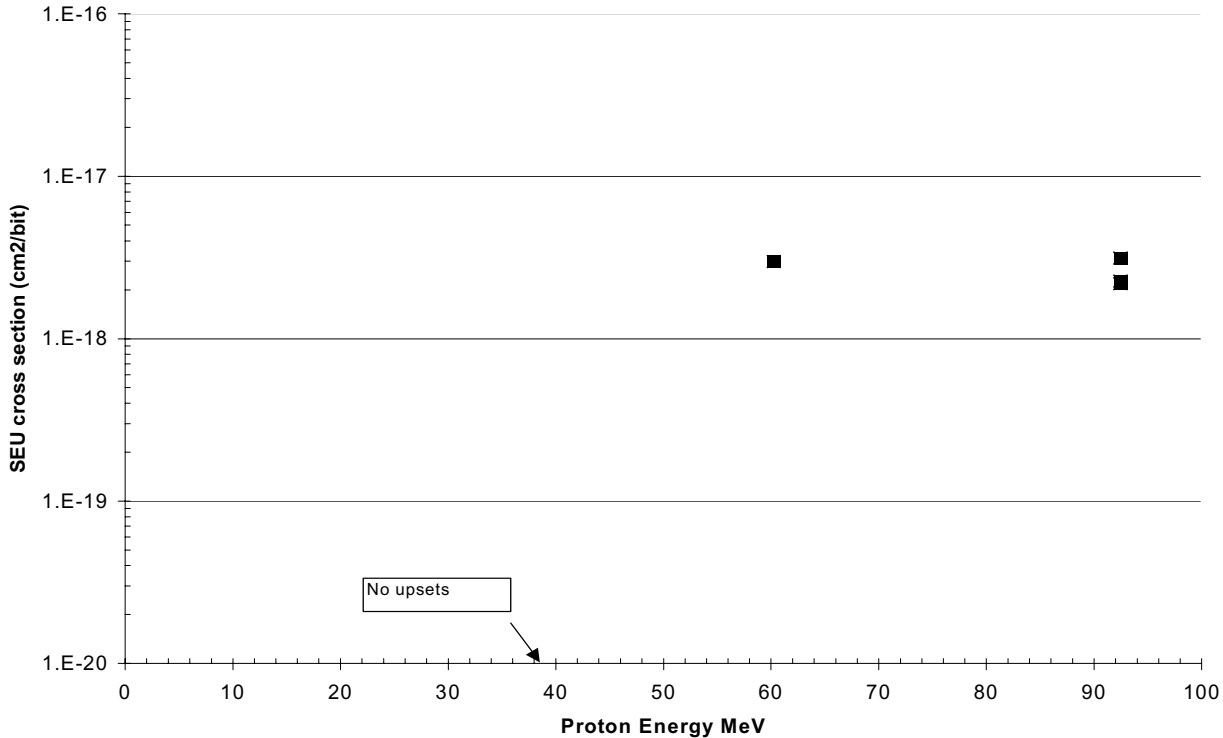


Figure 10. HIREX Proton SEU test data

approximately 3 E18 cm²/bit. One sample was exposed to proton total dose levels of around 14 krad (Si). Figure 10 shows the Proton cross-section. Since no MBU's were seen it is inferred that no SEFI's were seen. The part is not susceptible to latchups from protons.

SEE HEAVY ION DATA COMPARISON

Figure 11 plots SEU data from JPL, Aerospace, and Maxwell. A summary of these reports and other data taken by various organizations on this SDRAM die are included in Appendix B. The Aerospace data was converted to a per-bit cross-section assuming all 256 million bits were exercised. Because the lead frame was still on the Aerospace parts, it is uncertain if there are any additional errors that were not captured as a result of shielding. The JPL and Maxwell data is based on using parts programmed in the "inverse bleed down" pattern and both were collected at Texas A&M's Cyclotron. Aerospace's data was collected at Berkeley's Cyclotron.

Looking back at Figure 7, there is an order of magnitude difference in cross-section between the “bleed down” pattern and the “inverse bleed down” pattern. This could explain some of the discrepancies between Maxwell’s data as compared to that of Aerospace and JPL’s at higher LET’s, as well as, potential issues that may arise from shielding by the lead frames. As can be seen in the chart, there is a wide spread of data suggesting variations in testing methodology.

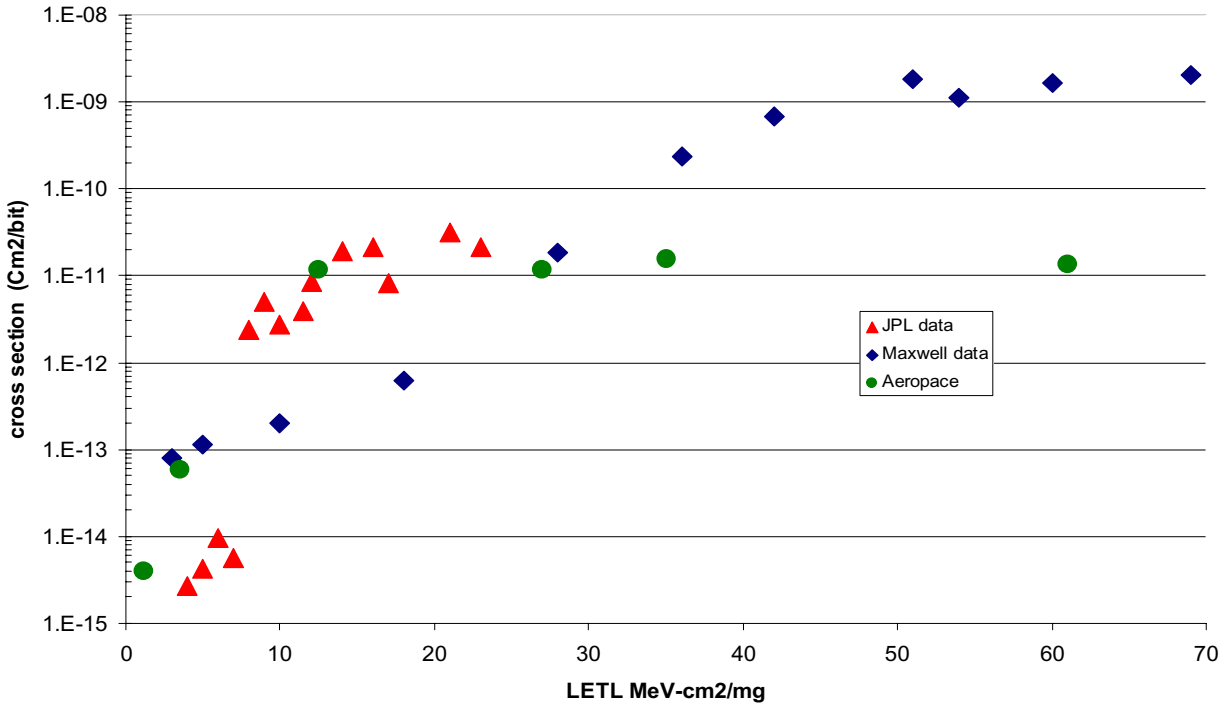


Figure 11. SEU Cross-section comparison from JPL, Aerospace, and Maxwell

ANALYSIS

A figure of merit for SEU, heavy ion rates has been developed by Petersen [9], based on a geosynchronous solar minimum environment.

$$R = 200x \frac{\sigma \bar{L}}{L_{.25}^2} \left[\frac{\text{upsets}}{\text{bit - day}} \frac{(\text{MeV / mg / cm}^2)^2}{\text{cm}^2} \right] \quad \text{Equation 1.}$$

Were $L_{.25}$ is the LET at 25% of the limiting cross-section and σ_L is the limiting cross-section. For SEL’s using the same figure of merit at the operating specification of 85 °C and assuming the threshold is 25% of saturation, the latchup threshold is 55 MeV-cm²/mg. This corresponds to a figure of merit latchup rate of 1.3 E-7 latchups/device-day or a latchup once every 20,000 year. Using the same method, the rate is once every 3000 year at 100 °C. Table 3 calculates the estimated latchup rate for various temperatures using two different methods: 1) Petersen’s figure of merit for SEU shown in equation 1, and 2) Space Radiation 4.0 modeling software for a geosynchronous orbit.

Temperature	SEL Threshold (MeV-cm ² /mg)	1) Petersen Figure of Merit		2) Space Radiation	
		SEL rate Latchups/day	SEL rate Years to Latchup	SEL Latchups/day	SEL rate Years to Latchup
50	85	5.5E-8	49800	2.8E-8	97800
60	69	8.4E-8	32600	5E-8	54800
70	60	1.1E-7	24900	7E-8	39100
80	57	1.2E-7	22800	8E-8	34200
90	53	1.4E-7	19200	1E-7	27400

Table 3. Latchup Estimates for Various Temperatures

The SEFI rate is dominated by Logic SEFI's whose saturated cross-section is 4 E-4 cm²/device, with a threshold of approximately 20 MeV-cm²/mg. In a geosynchronous orbit, the SEFI rate is 3.5 E-4 SEFI's/day or a SEFI every 8 years. The probability of a SEFI occurring is well within a typical geosynchronous mission. SEFI's have the added difficulty of creating thousands of errors simultaneously. Typical error detection and correction schemes cannot handle hundreds of simultaneous bit errors, so the probability of an uncorrected error is dominated by the SEFI rate.

For SEU's using the figure of merit above L₂₅ is 40 MeV-cm²/mg and σ_L 2 E-9 cm²/bit for the worse case inverse bleed down pattern. With this the error rate is 2.5 E-10 upsets/bit-day or 6.4 E-2 upsets/device day from heavy ions. Running a more detailed analysis with Space Radiation 4.0 and using Weibull function shape parameters of W equal to 50 and S equal to 6, the heavy ion rate is 1.2 E-13 upsets/bit-day or 3 E-5 upsets/device-day. This shows how using the step function method or the figure of merit can overestimate the SEU rate. Solar protons contribute another 6 E-12 upsets/bit-day or 1.4E-3 upsets/device-day based on the Hires proton test data. Therefore, the worst case SEU rate in a day during a solar flare would be the combination of the two rates or 1.4 E-3 upsets/device-day (dominated by the solar flares). Since the actual programmed pattern will be a combination inverse bleed down and bleed down pattern, the actual rate will be less. Rates in the proton belts found in lower orbits will be dominated by trapped protons and will be higher.

SEE MITIGATION

SEL

Analysis of a mission specific radiation requirement for SEL will include the part reliability requirements and the error rate. If the SEL rate is unacceptable for the mission requirements, there are several mitigation approaches that can be used. SEL is the most difficult single event effect to mitigate. Typical approaches involve power cycling the part or even the entire board. One method involves a design similar to Maxwell's LPT circuit, which would detect an increase in current and then shut down and re-power the memory. In testing of the SDRAM, the parts were shown to recover from latchup and continue to perform without degradation; however, these devices were all current limited by the tester. A second

approach would involve redundancy, which would require multiple SDRAM's that can operate with one or more parts non-operational. Yet another approach could include the nibble-wide Reed-Solomon error correction and detection scheme discussed below. In this case, there will be increased current consumption from the latched part and the error rate would increase because one nibble out of 12 would always produce an error

SEFI

To minimize SEFI induced errors, there are additional options than those that were discussed above for SEL. First, as demonstrated by the test, frequent setting of the mode register purges the memory of SEFI's.

To handle both SEFI's and SEU's, an error detection and correction scheme needs to be able to handle multiple bit or entire word errors throughout the whole device. An error code correction method used in Maxwell's next generation single board computer utilizes a Reed-Solomon routine. Each SDRAM represents one nibble of the 12-nibble address. In this configuration, 2 out of 12 SDRAM's can experience a complete memory failure and still be detected and fully corrected. The failure could be the result of an SEU, SEFI or an SEL. The uncorrected error rate is dependent on three nibble failures occurring within one scrub cycle. The overall error rate for a nibble correction scheme with individual error rate per scrub of *P* is:

$$=A \frac{n!(4xP)^3}{(n - m)!} \qquad \text{Equation 2.}$$

Where *n* is the number of SDRAM devices and *m* is the number of errors in an address that can't be corrected, in this case 3, and *A* is the number of addresses in the device. Using this scheme and a scrub rate of once per day, the SEFI error rate drops to 4.5 E-10 SEFI's/day. Because the scrub does not remove a SEFI, this method only works in conjunction with a MRS and when the MRS rate is higher than the scrub rate.

SEU

SEU can be addressed in the same method as discussed above. There are however more error correction routines that will work with SEU's than SEFI's. Some of those routines can be utilized on single SDRAM devices like a single bit EDAC scheme. Table 4 below compares the overall error rate for several different correction schemes based on a geosynchronous environment (including solar flares) and 2 Gigabits of memory.

No Correction	Single Bit EDAC <i>(Scrub 1/day)</i>	Reed Solomon Single Nibble Correction <i>(Scrub 1/day)</i>	Reed-Solomon Double Nibble Correction <i>(Scrub 1/day)</i>
4.1 errors/year	6E-3 SEU/year	1.7E-8 SEU/year	1.5E-20 SEU/year
.96 SEFI/year	1.08 SEFI/year	.18SEFI/year	1.6 E-7 SEFI/year

Table 4. Sample error correction schemes and corresponding error rates

The SEFI rate doesn't improve at all with a simple EDAC and actually gets worse because of the increased overhead (additional bits). The Reed-Solomon single nibble correction doesn't provide much improvement from SEFI's. In essence, the double nibble correct is required to have a major impact on the SEFI rate.

Since protons do not induce SEFI's, The SEFI rate will be worse in orbits with increased heavy ion fluxes, primarily the higher orbits including geosynchronous orbits. SEU will vary depending on the proton flux rate. Orbits in trapped proton belts will have higher SEU rates than outside the trapped proton belts. Solar flares will also affect the SEU rate, however these occur all at once so mitigation rates may be driven by solar flares.

STUCK BIT

Since stuck bits are temporary, a simple EDAC or other scheme should be able to detect errors induced by stuck bits. To correct stuck bits, the stuck bit has to have enough time to relax back to a programmable state. As mentioned earlier, 90% of the stuck bits returned to a programmable state after an hour of room temperature anneal time. Any correction schemes that require programming over these bits would need to allow for this anneal time. Because the stuck bits last less than a day, a correction scheme with a scrub rate of once per day, will correct most bits that have become stuck up to an hour before the scrub.

RECOMMENDED MITIGATION

The recommended mitigation approach for SEFI's, SEU's, and stuck bits is frequent MRS (higher than the scrub rate) and a double nibble detect and correct Reed-Solomon EDAC. The MRS will correct SEFI errors, while the Reed-Solomon double nibble correct will correct the SEFI induced bit errors and the SEU errors. Additionally, although the probability of an SEL is extremely small, the Reed-Solomon double nibble approach can still perform through a latchup although the correction performance will be degraded by the latched part. With this approach, if a latchup were to occur the dominant error would be SEFI's which would have a rate of 0.18 per year. The ability to power cycle the board would improve this by removing the latchup and returning the probability back to the double nibble rates shown in Table 3.

CONCLUSION

As a result of four heavy ion, single event tests performed by Maxwell, we have: 1) demonstrated that the Elpida 256 Megabit SDRAM die is the least susceptible to single event latchup and 2) fully characterized the 256 megabit Elpida SDRAM die for heavy ion induced single event effects. The SEL threshold is greater than 85 MeV-cm²/mg at room temperature (25 °C) and 55 MeV-cm²/mg at 85 °C. This corresponds to an SEL rate in a geosynchronous orbit (which is the worst case environment for heavy ions) of one latchup in 20,000 years when operating at 85 °C. The overall SEFI saturated cross-section is approximately 4 E-4 cm²/device, with a threshold around 20 MeV-cm²/mg. The overall SEFI rate in a geosynchronous orbit is once every 8 years. The SEU inverse bleed down (worse case SEU) saturated cross-section is 2 E-9 cm²/bit, with a SEU threshold of approximately 2.7 MeV-cm²/mg. This corresponds to an upset rate of approximately 3 E-5 per day in a geosynchronous orbit. The proton cross-section at 92.5 MeV is approximately 3 E18 cm²/bit. The part is not subject to multiple bit upsets from protons.

Mitigation methods for the various radiation effects include: 1) SEL—power cycling, redundancy and Reed-Solomon, 2) SEFI—MRS and Reed-Solomon double nibble detect and correct EDAC, 3) SEU—most error detection and correction schemes and finally, 4) Stuck Bits—can be easily detected, but require a period of time before they can be corrected based on the relaxation time shown in Figure 9. For the majority of missions, the recommended mitigation scheme would include frequent MRS coupled with a Reed-Solomon EDAC.

Utilizing a double nibble detect and correct Reed-Solomon EDAC, the single event error rate drops to once every 6 million years. The overall error rate including those caused by single event latchups is $1E-5$ uncorrectable errors/year.

Although the SDRAM is a complex part, through detailed characterization and the use of EDAC mitigation schemes, the Elpida 256 Megabit SDRAM die is a good candidate for space applications requiring the highest performance, highest density volatile memory.

APPENDIX A

DEFINITIONS

CAS	Column Address Strobe
DUT	Device Under Test
EDAC	Error Detection and Correction
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
MRS	Mode Register Set
PCB	Printed Circuit Board
RAS	Row Address Strobe
SDRAM	Synchronous Dynamic Random Access Memory
SEU	Single Event Upset
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latchup
TAMU	Texas A & M University Cyclotron
TID	Total Ionizing Dose

APPENDIX B

SINGLE EVENT EFFECTS

Aerospace [1][2][3]

Aerospace Corporation performed heavy ion and proton testing on a variety of 256 Megabit SDRAM devices. Their test showed that SEL thresholds from both Samsung and IBM were below 40 MeV-cm²/mg, while the Hitachi (now Elpida) had a SEL threshold of greater than 61 MeV-cm²/mg, having accumulated 1 E7 particles/cm². Aerospace also found that there were increasing multiple bit upsets (MBU) correlating with increasing LET values, as shown in Figure B-1. The upper curve (squares) labeled 'upset bits total' represents the total number of bit errors including those induced by SEFI's. The lower curve (diamonds) labeled 'SEE events' shows the total number of SEE events and does not count each upset independently of the multiple bit upsets, thereby, representing a quasi SEU cross-section which includes SEFI events. This would correspond to a saturated SEU cross-section of 1.4 E-11 cm²/bit.

With respect to SEFI's, Aerospace found that there were different types; some that created multiple errors and some that are considered more major; encompassing many consecutive

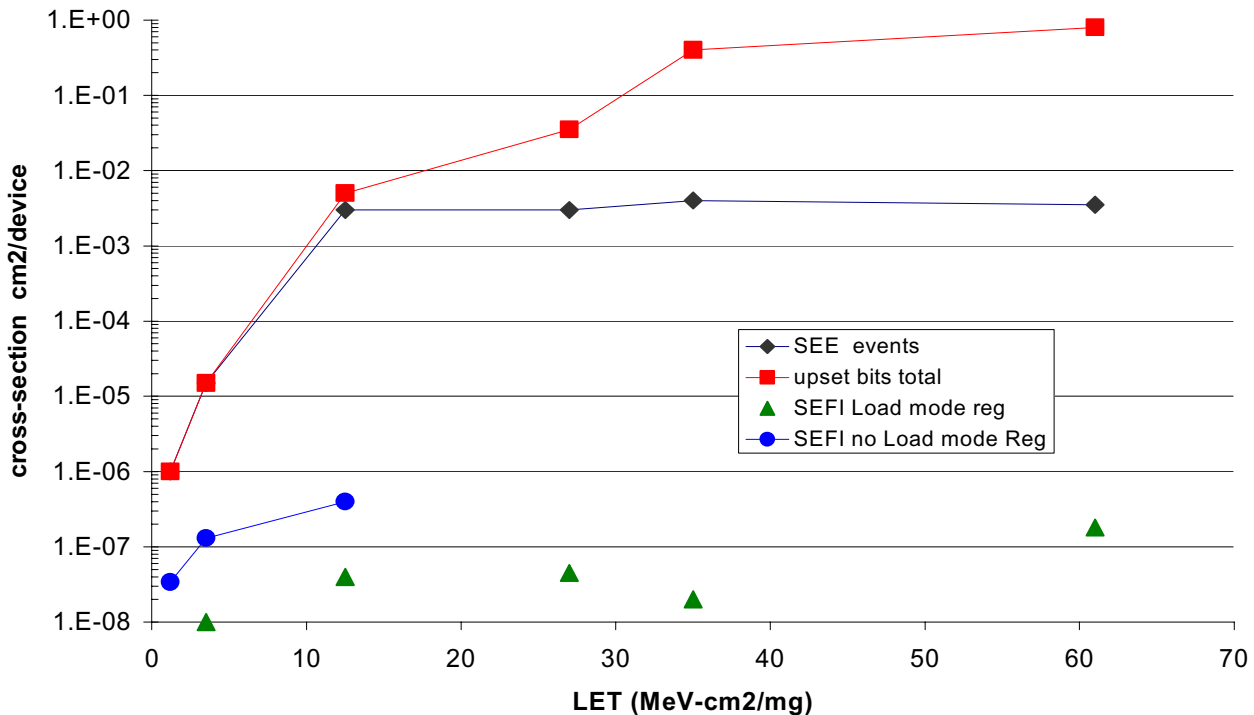


Figure B-1. Aerospace heavy ion SEE data upsets and SEFI

address locations [1]. When reloading the mode register, the SEFI rate was lowered, by about an order of magnitude when compared to not reloading the mode registers (see the lower two curves in Figure B-1). For protons with energies up to 200 MeV, in the read mode the SEU saturated cross-section was approximately 4 E-9 cm²/device. While in a precharge,

autorefresh, Load Mode Register and Idle state, the saturated cross-section was about $9 \text{ E-9 cm}^2/\text{device}$. No SEFI's were seen with protons in either the read mode or the precharge, auto-refresh, load mode register and idle down mode. Aerospace also saw stuck bits that were a function of both the LET of the ion and the time period after irradiation. They concluded that this effect is a collective result of the ions, as opposed to that caused by an individual ion. There were 4 to 18 stuck bits from less than $1 \text{ E5 particles/cm}^2\text{-sec}$ and several krad (Si). They annealed out in about 10 minutes after removal of the ion source.

Aerospace (RADECS 2001 report) [10]

Aerospace irradiated the Hitachi device at 5.5 rad/sec. At 20 krad(Si) they did not observe any stuck bits. Four stuck bits were seen after 40 krad(Si), 188 stuck bits after 60 krad(Si).

JPL 2001 [6], [7]

JPL performed heavy ion radiation test of the Hitachi 256 Megabit SDRAM. This test used the inverse bleed down pattern or the state inverse of the state where the memory cell returns to when it is not refreshed or the relaxed state. These tests were performed at room temperature ($25 \text{ }^\circ\text{C}$). In addition, the tests were run with devices in the standby state with a known pattern. Figure B-2 shows the SEU cross-section that was generated from averaging the data from two devices, as reported in the JPL report. Both devices had a rapid increase in the SEU cross-section around 7 and 8 $\text{MeV-cm}^2/\text{mg}$.

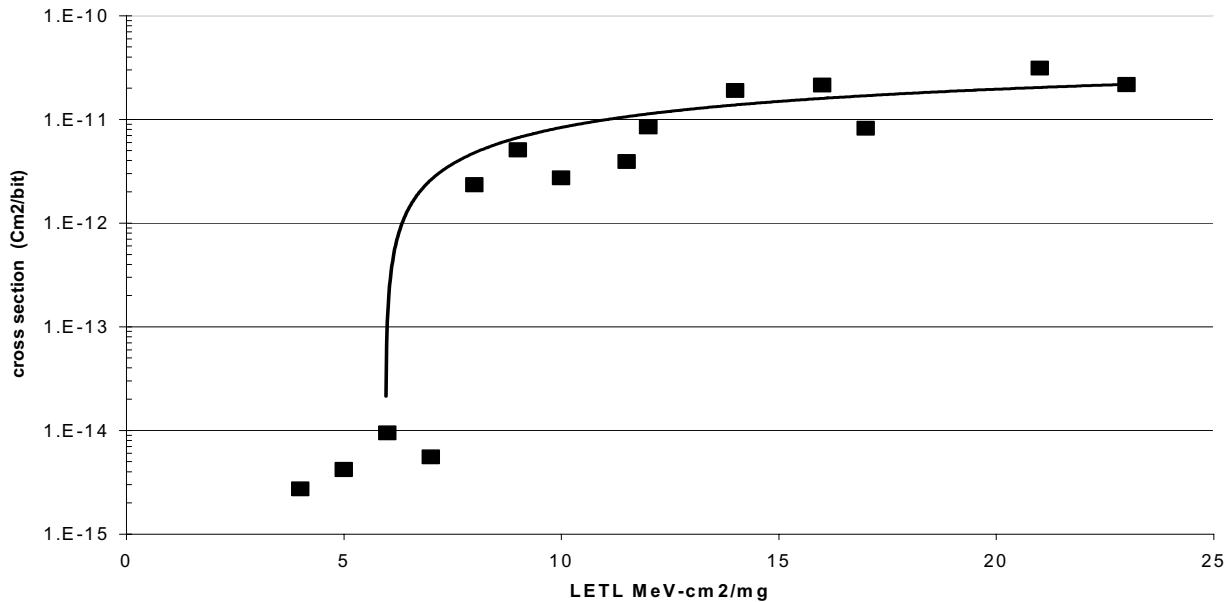


Figure B-2. JPL SEU cross-section Inverse bleed down pattern

UTMC July 2002 [8]

UTMC performed heavy ion testing of the Hitachi 256 Megabit device at Texas A&M's Cyclotron facility. They established an SEL threshold of greater than $60 \text{ MeV-cm}^2/\text{mg}$ at an elevated temperature of $85 \text{ }^\circ\text{C}$ (total fluence of $5.6\text{E} 6$ without Latchup). Furthermore, they observed latchups between 40 and $60 \text{ MeV-cm}^2/\text{mg}$ at $100 \text{ }^\circ\text{C}$.



UTMC reported three types of errors: 1) mode register corruption requiring reloading the mode registers, 2) self correcting burst of errors in a single read cycle and 3) SEU's. The cross-section for UTMC's data actually goes down at higher. They had one data point at 30 MeV-cm²/mg, which if discarded would give a saturated cross-section of approximately 2E-12 cm²/bit. The self-correcting, burst mode error saturated cross-section is approximately 7E-6 cm²/device and the errors requiring a mode register reset is approximately 8 E-6 cm²/device.

APPENDIX C

REFERENCES

- [1] R. Koga, S. H. Crain, P. Yu and K. B. Crawford, "See Sensitivity Determination of High-Density DRAMs with limited-Range heavy ions", IEEE NSREC Data Workshop Record pp 45 – 52, 2000.
- [2] R. Koga, P. Yu, K. B. Crawford, and S. H. Crain, "Permanent Single Event Functional interrupts (SEFI's) in 128- and 256 Megabit Synchronous Dynamic Random Access Memories (SDRAMs) ", IEEE NSREC Data Workshop Record pp 6 – 13, 2001.
- [3] R. Koga, P. Yu, K. B. Crawford, S. H. Crain and V. Tran, " Comparison of heavy ion and Proton-Induced Single Event Effects (SEE) Sensitivities," IEEE Trans. Nucl. Sci., vol. 49, No. 6, Dec 2002, pp 3135-3141
- [4] B. Pritchard, G. Swift, A. Johnston, "Radiation Effects Predicted, Observed, and Compared for Spacecraft Systems", IEEE NSREC Workshop Record 2002, PP. 7-13.
- [5] J.G. Loquet " Proton Single Event Effects Radiation Test Report", Hirex report HRX/SEE/043 dated February 18, 2002 for Hitachi HM5225805.
- [6] L. Scheick " SEE Measurement of SDRAMs" December 1999 released 2002 on JPL's radnet Website.
- [7] L. Edmonds, S. Guertin, L. Scheick, D. Nguyen, and G. Swift, " Ion Induced Stuck Bits in 1T/1C SDRAM Cells. JPL report.
- [8] J. Benedetto, "Radiation Effects Qualification of an Advanced Synchronous Dynamic Random Access Memory (SDRAM), UTMC report July 2002.
- [9] E. Petersen, "Single event analysis and prediction", 1997, IEEE NSREC Short Course Section III.
- [10] R. Koga, S. Crain, K. Crawford, and P. Yu, " Heavy ion induced Hard Errors in Memory Devices with Sub-micron Feature Sizes" RADECS 2001 conference proceedings.